

Model Name: GA-Z87-D3H

1.02

SHEET

TITLE

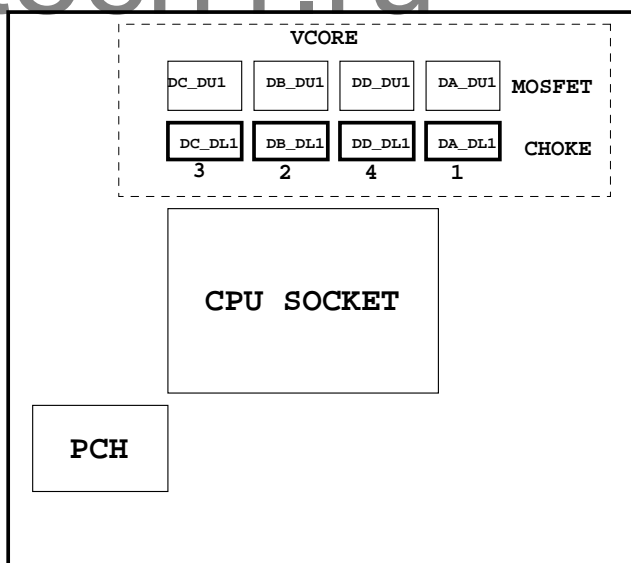
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564b
24	VCORE+DDR PWM IR3553+IR3598
25	ME POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	LAN INTEL i217
32	DVI
33	HDMI , R_USB30
34	TABLE LIST
35	
36	
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Gigabyte Technology

Title			
Cover Sheet			
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GA-Z87-D3H

Component value change history

Data	Change Item	Reason
0.1-0925	E-BOM	
	1. Z77-D3H改為削光黑PCB, slots同原本削光黑機種配色, CPU socket鍍黑	
	2. 8 series IR digital power PWM因Intel spec change, 須改用b版 (必須發行Firmware)	
	3. H77-D3H 注意上H87 chips, 上ME power, 咖啡黑機種配色,	
	3. H77-D3H GPIO37 需Pull up to 3VDUAL	
0.2	1. Load-line DAR47 2.06K --> 2.37K , DAR46/50 1.4K --> 1.6K , DAC17 150P --> 100P	
	2. N_-LAN_WAKE NR60 8.2K/4 --> 1K/4/1	
	3. DA_DUI, DB_DUI, DD_DUI, DC_DUI 10IFB-403553-01R --> 0TA1-603551-00R	
	4. DDR CHOKES阻值調整	
	5. CPU SOCKET + RM 要用新料號?	
0.2B	1. 確定Power stage用料:IR3553 or IR3550 or 3551?	
	2. GPIO8 "NR136"不上	
	3. Add +12V排阻 RN2-RN6	
0.2C	1. HU1 , HU2 level shifter change to NXP	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
	3. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak	
1.0	1. PCIE X16 patch reset circuit 怎麼上?	
	2. Prochot是否只上一組	
	3. PCH_HS & MOS_HS change new 料號	
	4. 因DII 2222禁用, 注意Z87-D3H試產時用Panjit 2222是否可用(BOM已內建)	
	5. HDMI/DVI change to NXP level shifter	
	6. CHECK 5VSB保護線路是否上件	
10A	1. PCB REV1.0 --> REV1.01	
	2. Update LAN: i217V料號	
	3. Add DAQ6, DAR81	
10B	1. Add M3 POWER For Remote wake on LAN	
10C	1. Remove DAJP1	
	2. 5VDUAL OVP --> 5VSB OVP	
	3. Remove 全成信PCB	

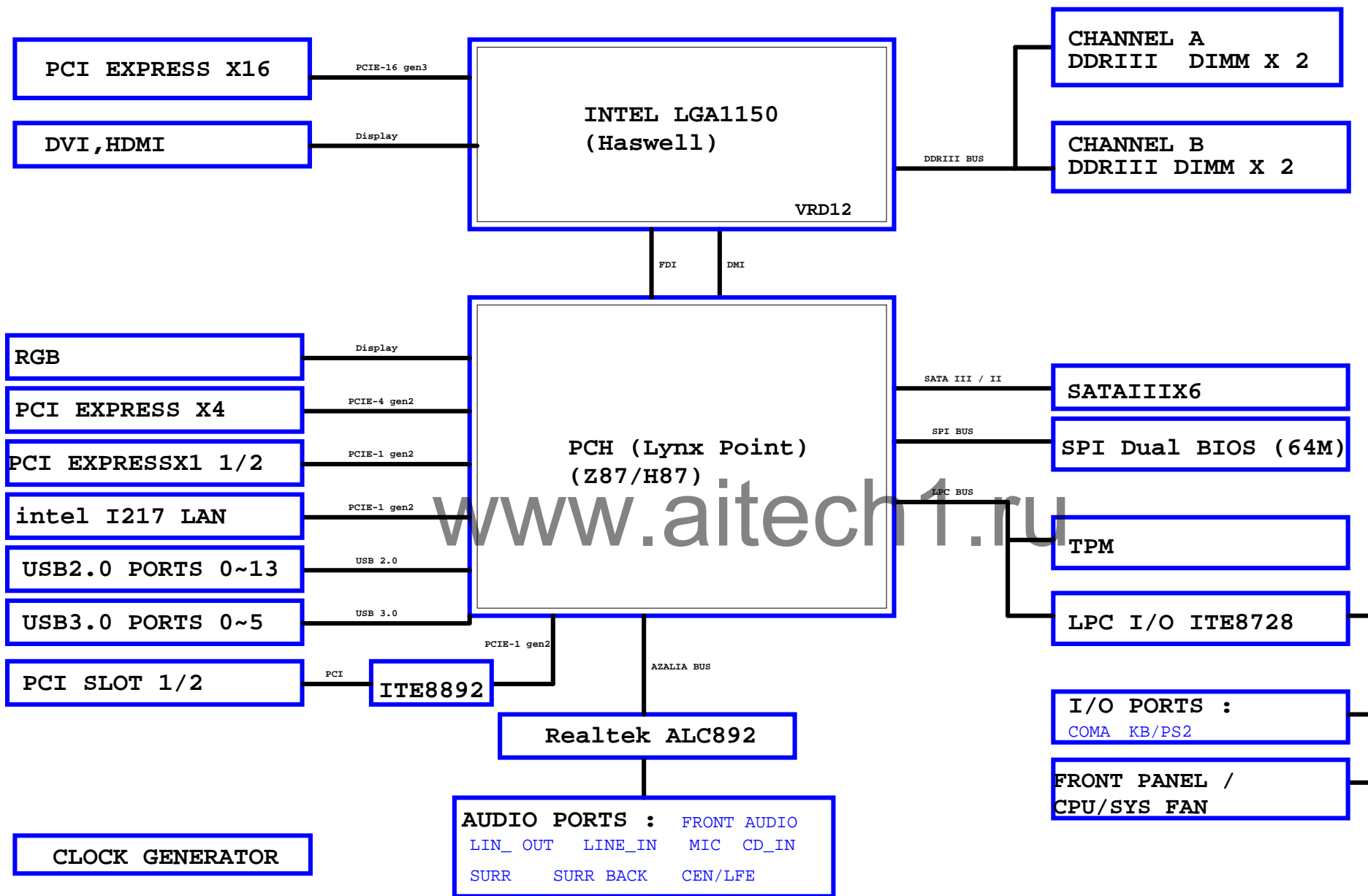
Circuit or PCB layout change

DATE	Change Item	Reason
0.1	E-BOM	
0.2	1. U8 pin3加粗40mils 2. Update LAYOUT NEW RULE for四層板 3. MDA6線長T型要繞等長 4. N_GPIO37 pull up VCC3 --> 3VDUAL 5. CPU Thertrip CPU_VTT --> VCC1_05_PCH 6. 確認 R/G/B ESD擺放位置 7. Add PCIE X16 reset patch circuit 8. PCIE signal by group 成對走 9. VIN0 --> VCORE0 , VIN5 --> VCORE 10. CS 1pin --> 2pin 11. 後窗部份鋪銅會挖 + 字處理 12. Add MA_DR8 , MA_DC8單獨下地 13. add VTT_PWRGD control circit 14. Update F_PANEL footprint "H2X10PANEL-3" 15. NR132跟NC59 layout位置交換 16. Add DS_ME GP67 control 17. Q6位置靠近 PWM power control pin 18. WR59 change to "R0204-2" 19. 文字面 "DualBIOS" , 改為" Dual UEFI BIOS" , Add "Intel GbE LAN" 20. MAU2 REF "GND" 21. DDR Choke ML1, ML2 1.2uH/20A --> 0.8uH/35A	
0.21	1. AUDIO SPDIF-IN CR77 "0402-2" FOR short protection 2. add AUDIO ON/OFF PLAYER 3. Change PCIE X1/PCIE X4 CLK 4. Update F_PANEL footprint 5. CPU VRIN OV IO_GP81 --> IO_GP21	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
1.0	1. 0 ohm --> short pad 2. 簡化CPU Config setting 3. 預留N_PCH_DPWROK 控制線路 4. 注意Slot和後窗正面有做十字Thermal處理 5. NBC65移靠近PCH 6. Add R700-R702 for FAN short protection 7. PWR_LED 改為IO_GP65 8. VTT_PWRGD Update 9. N_GPIO37 pull-up to VCC3 10. +12V RN2-RN6 & VCC/VCC3/5VSB dummy load 排阻 11. DDR_15V H/W monitor detect 改從 DDR slot 拉回 12. 5VSB AD1要過 NET 13. DDR VIN 間隔拉開 , 背板GATE往上移 14. Add DDR_15V dummy load 15. 5VSB/5VDUAL OVP protection	
1.01	1. 0 ohm --> short pad 2. Remove "BIOS_PH" & "M_BIOS socket" & "CS" pin 3. Add MADQ6 4. USB3 port3/4 , 5/6 swap	

1.02	1. CPU_FAN ADD 100UF 2. DART2改成R0402-2(靠近DD_DUI) , DART4改成R0603-RH(放在DART2左邊) , RS1改成R0402-2 3. Add DAR82 For MOSFET "PHSFLT-" protect	
1.03	1. ALL FAN ADD 0.1u/4 2. 文字面UEFI DUALBIOS 3. USB3.0/Intel GbE LAN/HDMI/DVI文字面移到MOS_HS外面 4. HDMI update "HDMI-3"	

Gigabyte Technology			
BOM & PCB MODIFY HISTORY			
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# BLOCK DIAGRAM



LGA1150 (D)



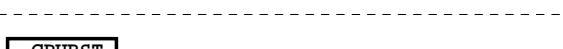
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**LGA1150 (D)**



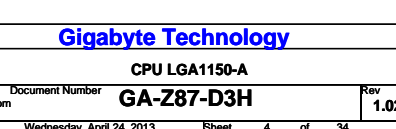
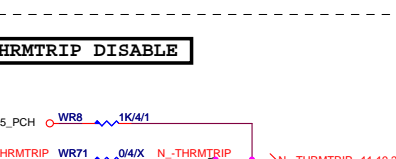
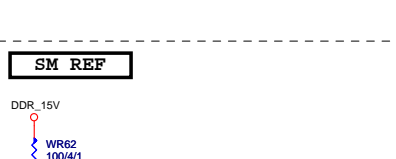
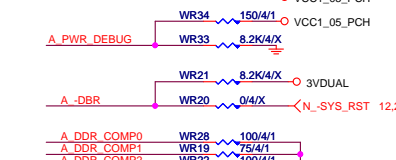
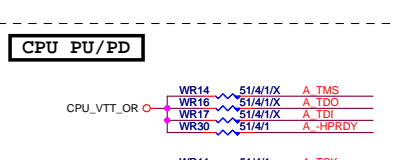
1111

PA\_EXP\_RXP[0..15] >> PA\_EXP\_RXP[0..15] 14

PA\_EXP\_RXN[0..15] >> PA\_EXP\_RXN[0..15] 14

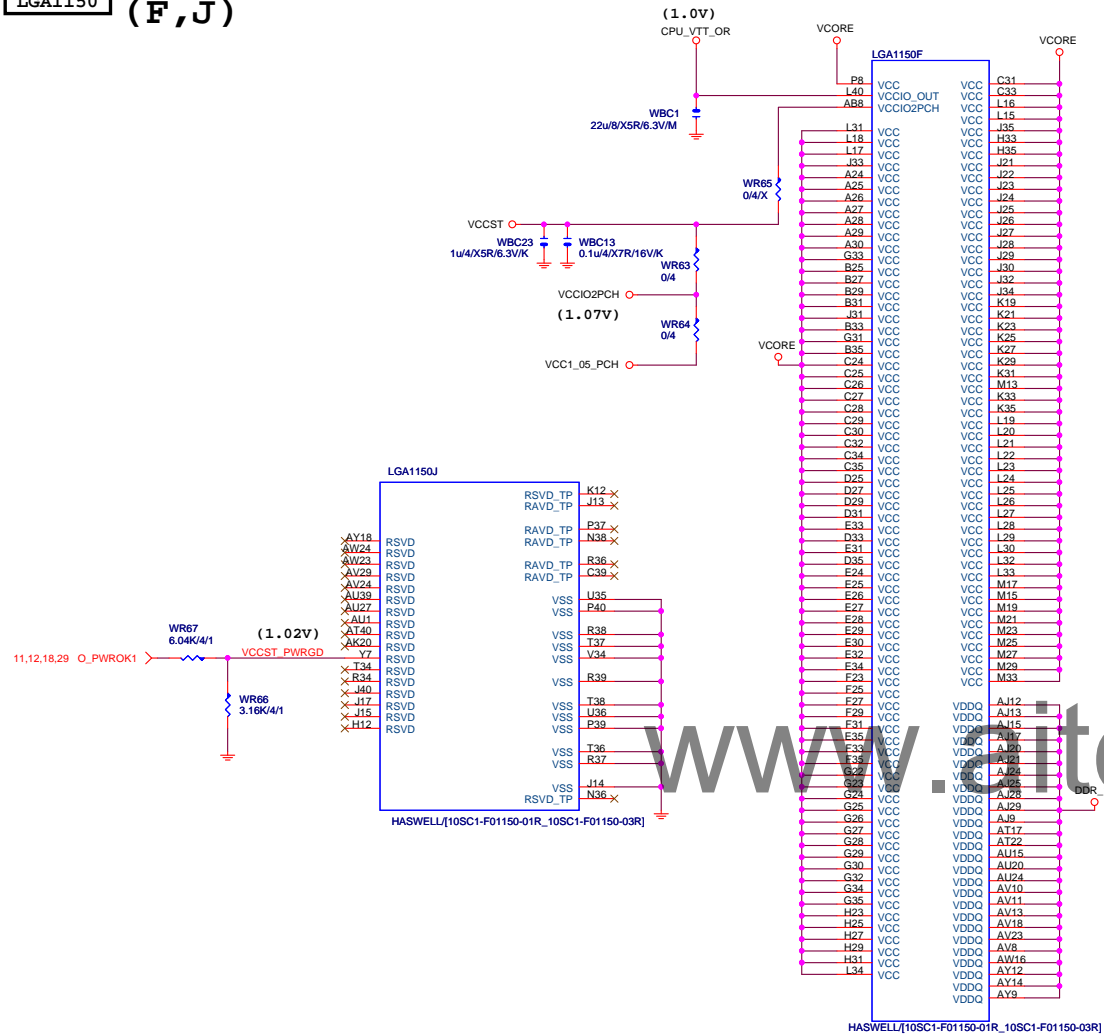


SM REF
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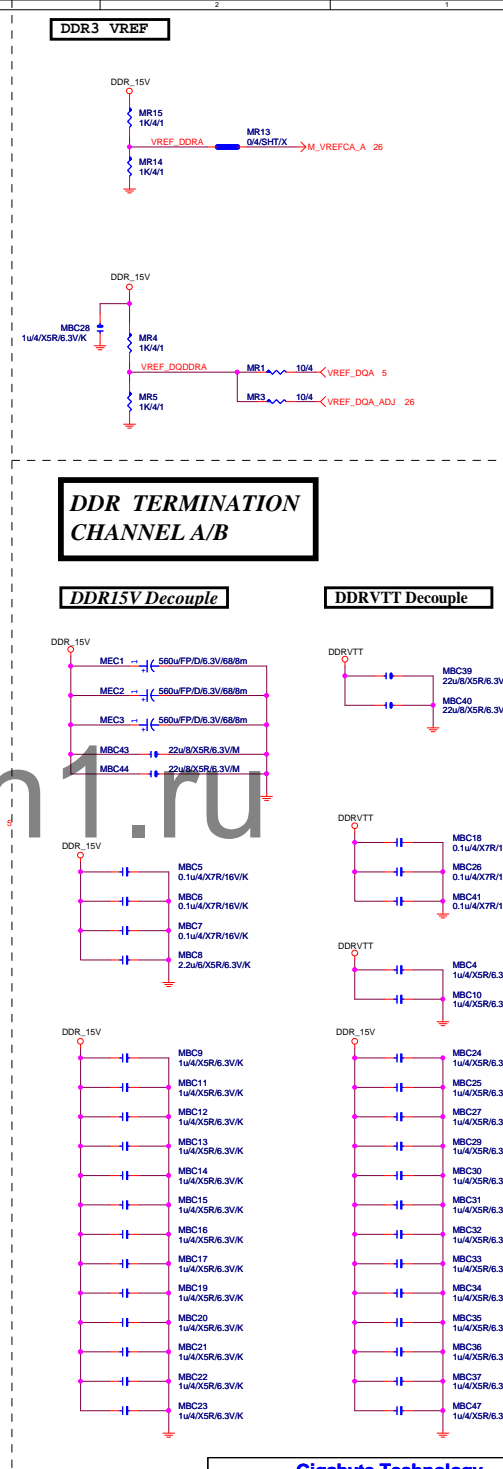
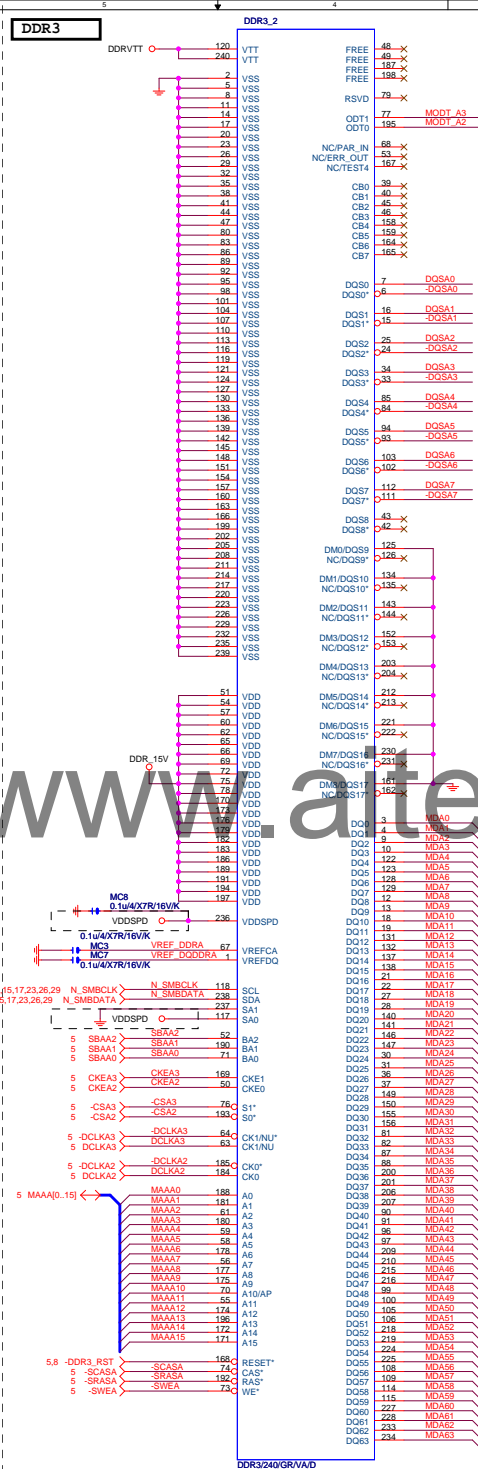
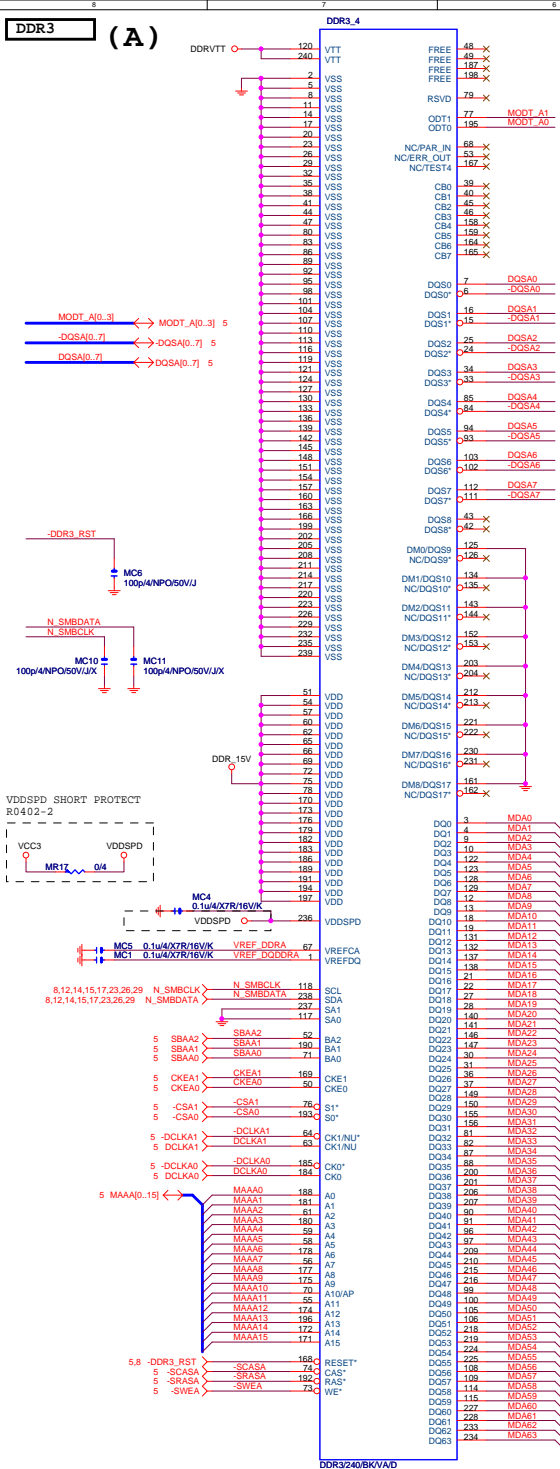
# LGA1150 (F,J)

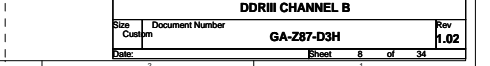


# LGA1150 (G,H,I)







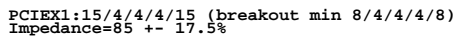




DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

PCHB

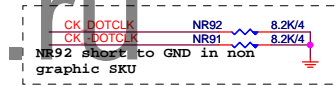
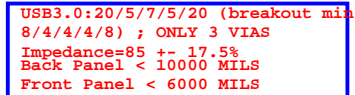
B85: Port 6/7 N/A  
H81: Port 6/7/12/13 N/A



usb2.0 12/5/7/5//12

usb3.0 20/5/775/720  
=====

28 PCH\_USB3\_RXN0 > F20 USB3 USB3\_RXN\_0 FDI\_RXN\_0 N1

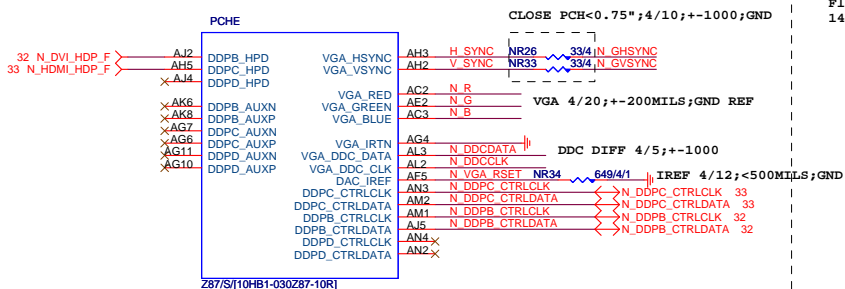


Z87/S/[10HB1-030Z87-10R]

PCH\_HS/[12SP2-S06012-11R\_12SP2-S06012-12R\_12SP2-S06012-13R]

Title			
PCH FDI,DMI,USB ,PCIE			
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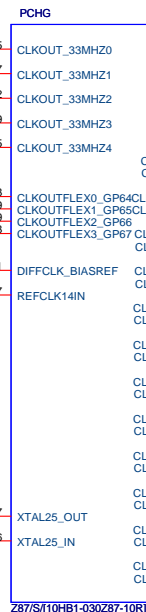
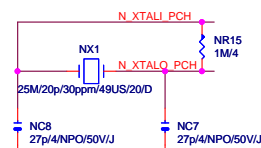
# PCH (E)



VGA DISABLE	
R,G,B	NC OR GND
IRTN / IREF	GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA	NC
POWER VCCADAC(AF2), VCCADACBG(AE1)	GND

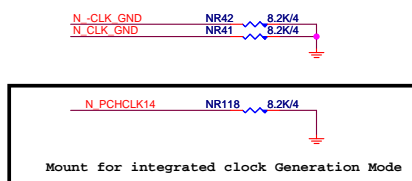
# PCH (G)

Flex1,2,3,4 : 14/24/33/48MHz



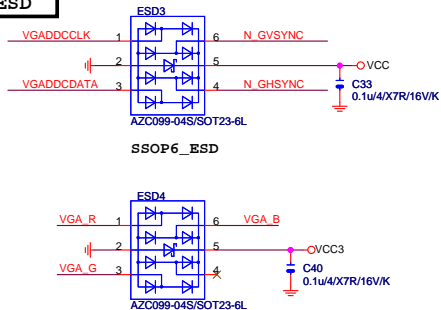
Differential Clock:15/4/6/4/15 Impedance=90 +- 15%

## PCH CLK PD

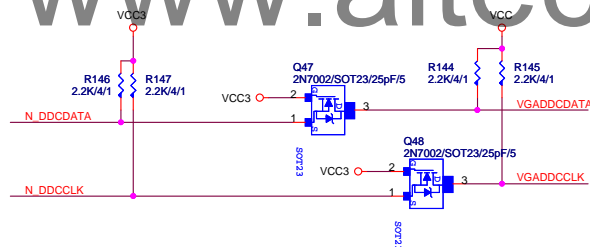


Mount for integrated clock Generation Mode

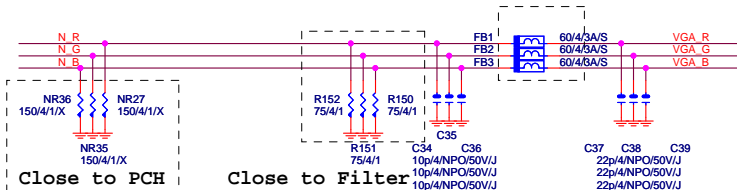
## VGA ESD



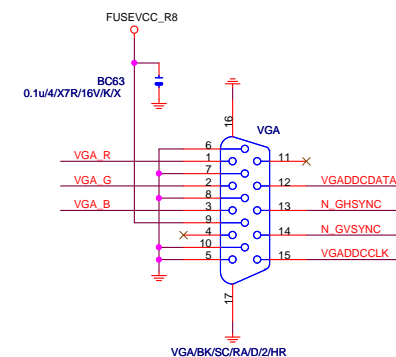
## VGA DDC



## VGA DDC



## VGA CONNECTOR

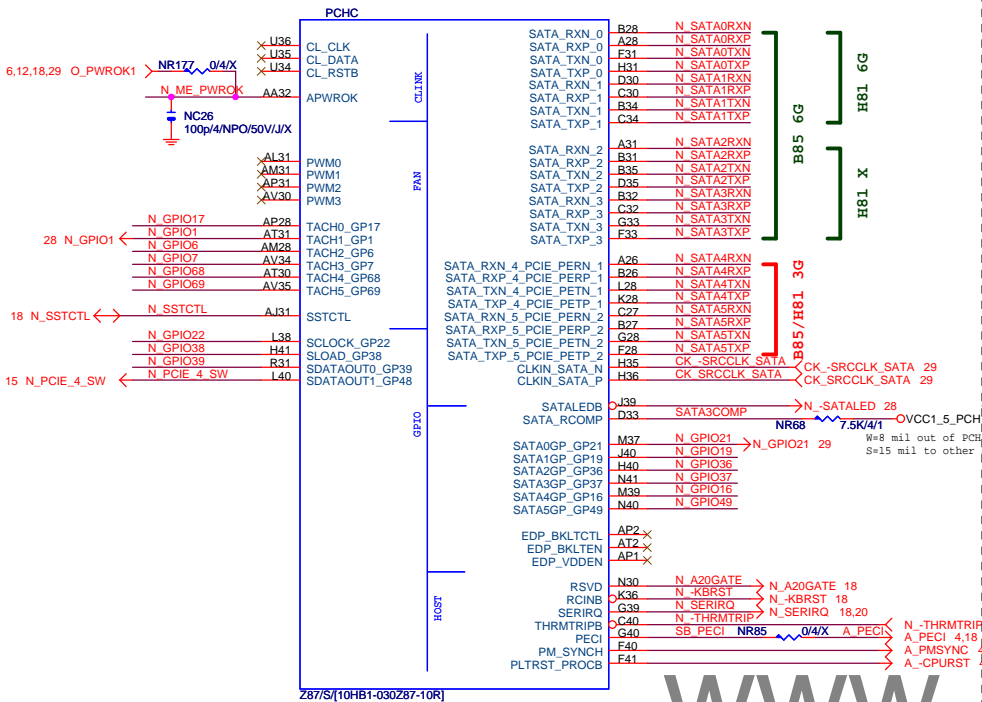


## Gigabyte Technology

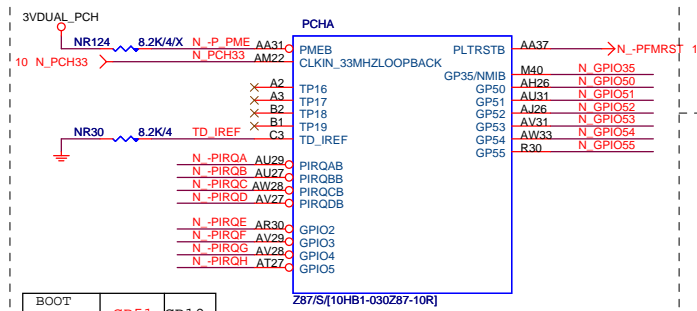
Title			PCH DISPLAY ,CLK BUFFER	
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# PCH (C)

SATA3 : 20/4/4/20 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

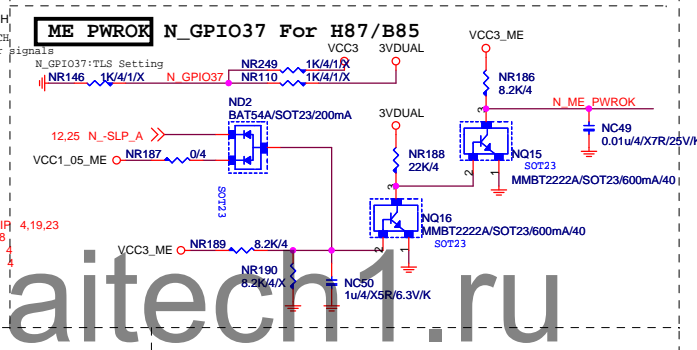


# PCH (A)

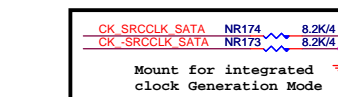


BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	1	1

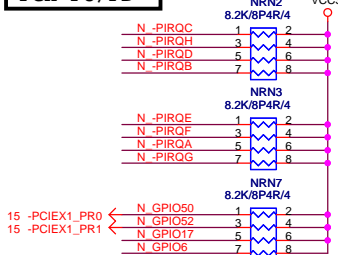
Default int pull up on GP51,  
Default SPI boot devices



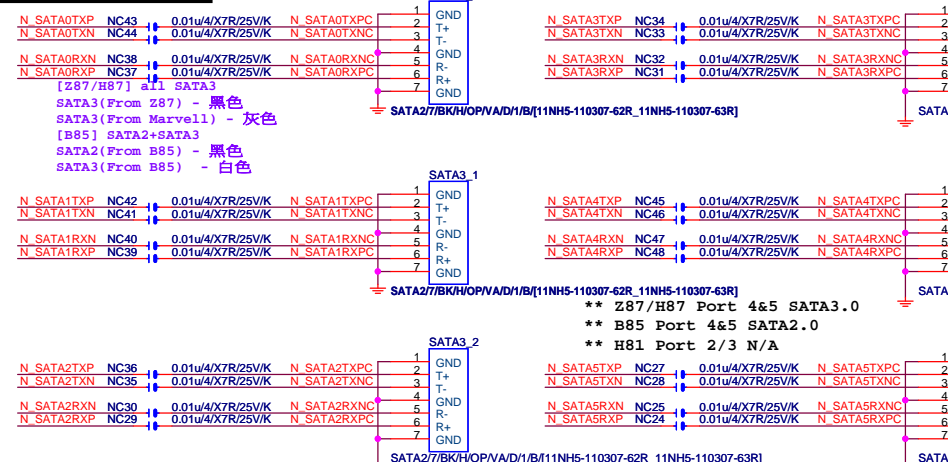
# PCH CLK PD



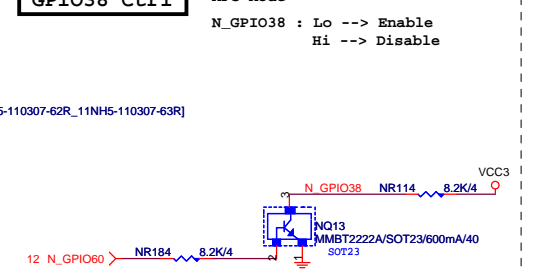
# PCH PU/PD



# SATA3 CONNECTOR



# GPIO38 Ctrl

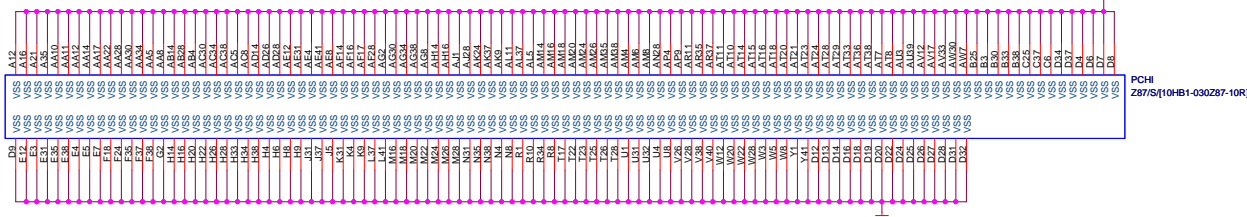


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PCH HOST , SATA, PCI		
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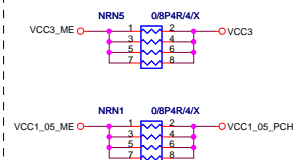
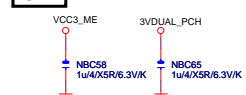


**PCH (I)**

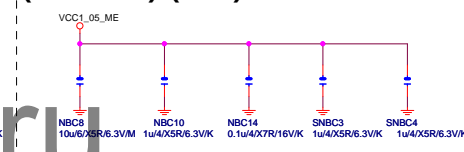


SHT PWR

CAP



(1.05V) (x5)

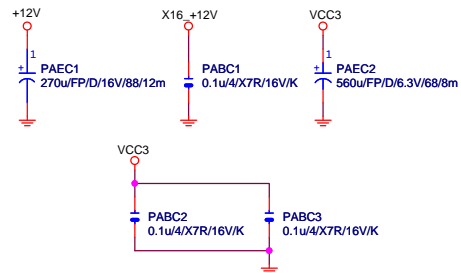


(1.05V)(X2) (3.3V) (X2)



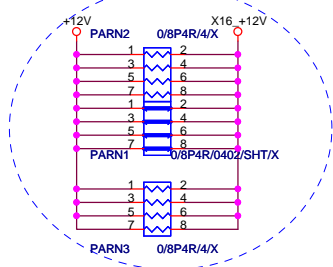


## PCIEX16 CAP



## PCIEX16 PROTECT SHT

```
+12  protect
short-wire test
```



PCIEX16	AC	CAP
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PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXP1	PAC4	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXP1	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAc7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAc9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAc10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAc11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAc12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAc13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAc14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAc15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAc16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAc17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAc18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAc18	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAc20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAc21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAc22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAc23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAc24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAc25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAc26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAc27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAc28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAc29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAc30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAc31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAc32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAc33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAc34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAc35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

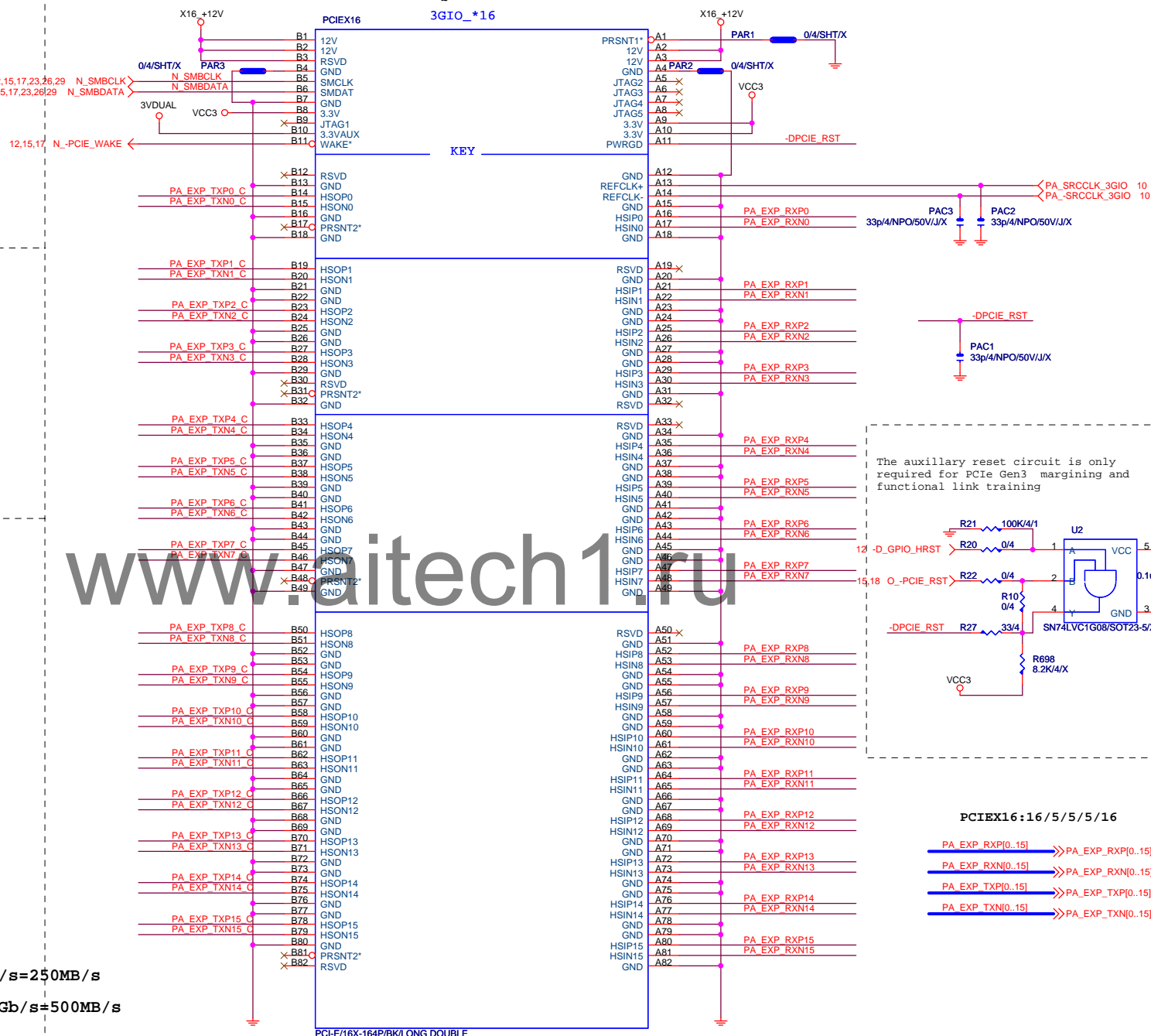
PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

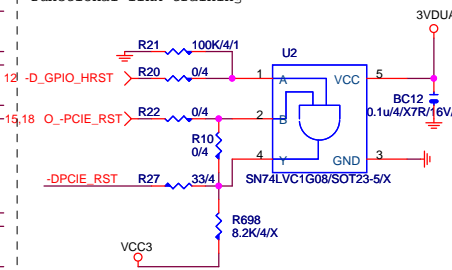
PCI-E REV:2.0--&gt; 5GHZ

## PCIEX16 SLOT

PCIESLOT-164DN-Q



The auxillary reset circuit is only required for PCIe Gen3 margining and functional link training.



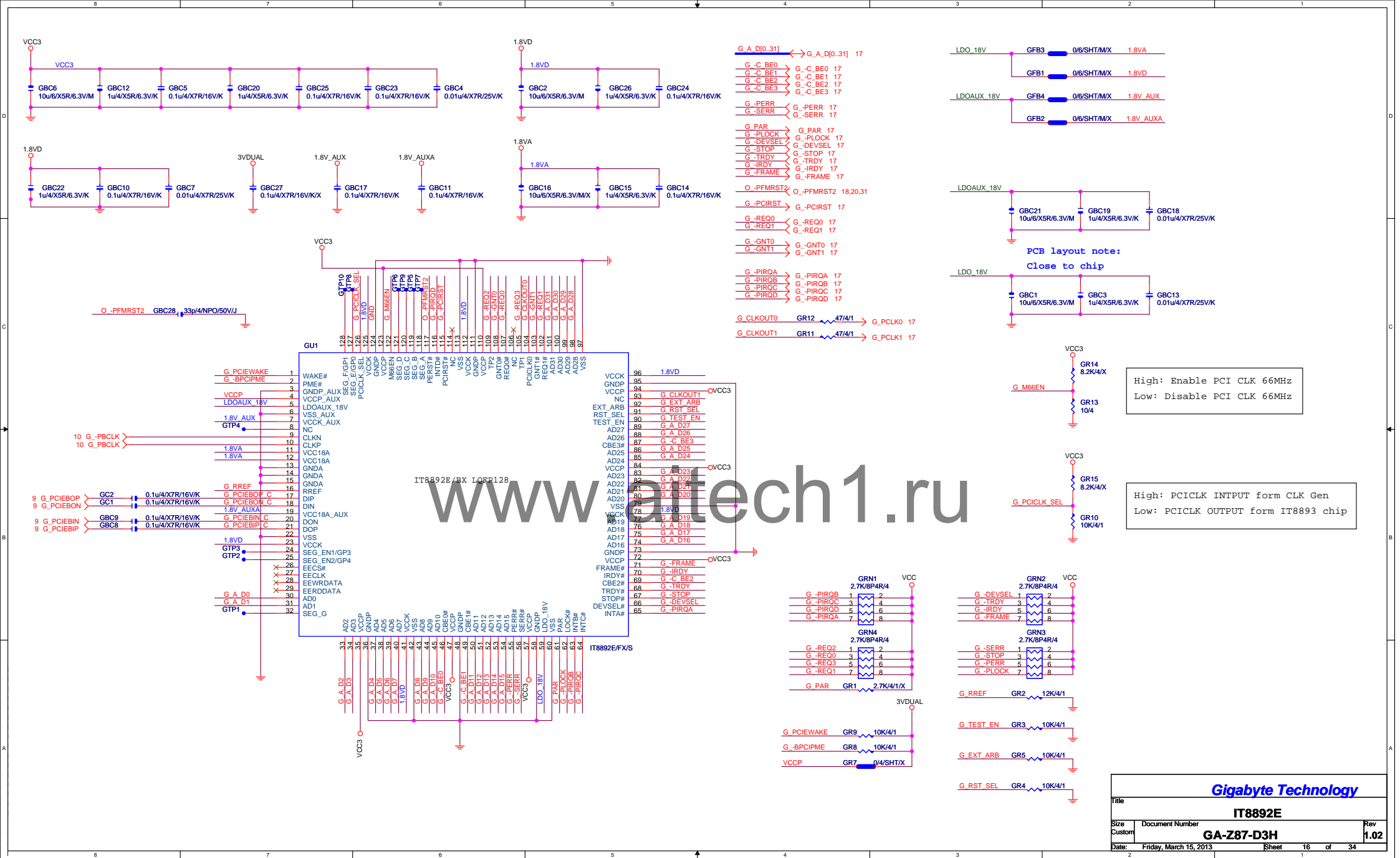
PCIEX16:16/5/5/5/16

PA_EXP_RXP[0..15]	>>	PA_EXP_RXP[0..15]	4
PA_EXP_RXN[0..15]	>>	PA_EXP_RXN[0..15]	4
PA_EXP_TXP[0..15]	>>	PA_EXP_TXP[0..15]	4
PA_EXP_TXN[0..15]	>>	PA_EXP_TXN[0..15]	4



	N_PCIE_4_SW (PCH_GPIO48)	PCIEX4_X1 (SIO_GPIO26)
PCIEX1,PCIEX4 --> X1 ( Default )	H	H
PCIEX4 No devices PCIEX4 -> X1	H	H
PCIEX4 Have devices PCIEX4 -> X4 PCIEX1_1/2 --> N/A	L	L

[illegible]



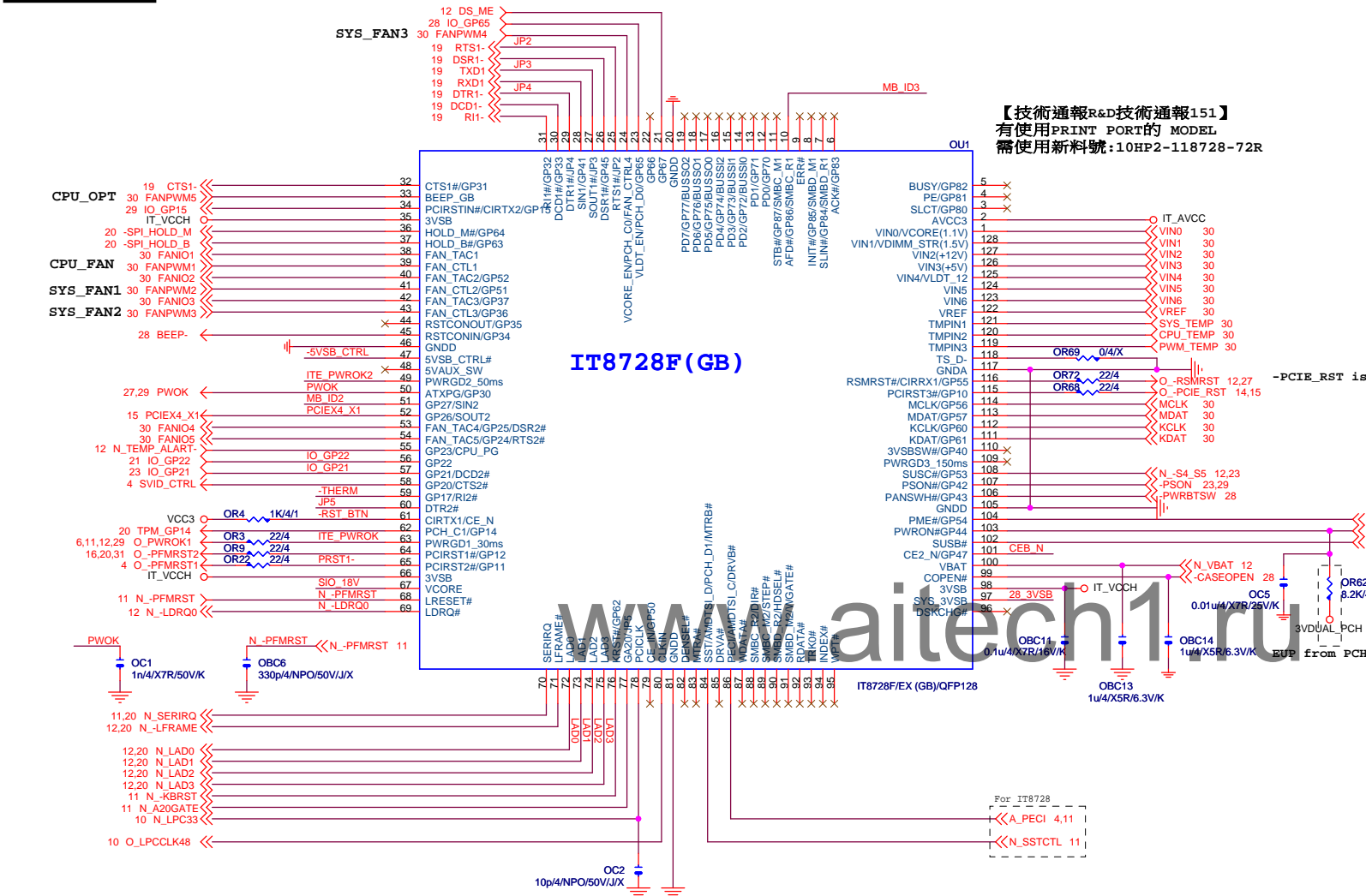
High: Enable PCI CLK 66MHz  
Low: Disable PCI CLK 66MHz

High: PCICLK INPUT form CLK Gen  
Low: PCICLK OUTPUT form IT8893 chip

Gigabyte Technology		
File		
IT8892E		
Size	Document Number	
	GA-Z87-D3H	
Date:	Friday, March 15, 2013	
	Sheet	16 of 34
Rev 1.02		

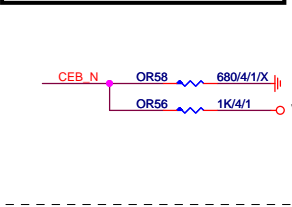


# SIO IT8728F

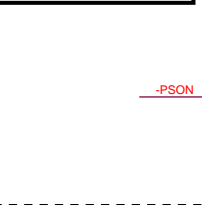


IT8728F NOTE	
PIN121	VCORE_EN/PCH_C0
PIN120	VLDT_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSL_D/MTRB#/PCH_D1
PIN55	PCI/AMDTSL_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

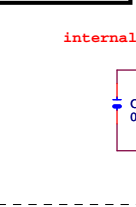
## DUAL BIOS OPT STRAP



## Power leakage



## SIO\_18V



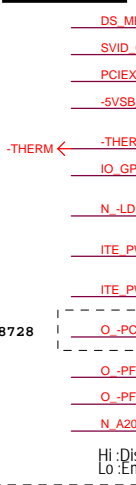
## SIO CAP



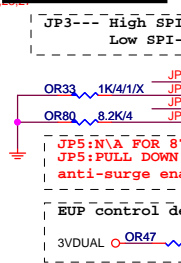
## PWR SHT



## SIO PU



## SIO STRAP



JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

## MB ID



**Gigabyte Technology**

Title

ITE 8728 LPC IO

Size B

Document Number

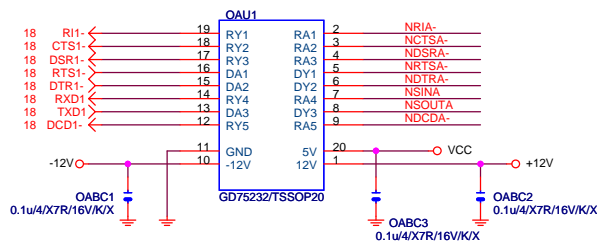
GA-Z87-D3H

Date: Friday, March 15, 2013

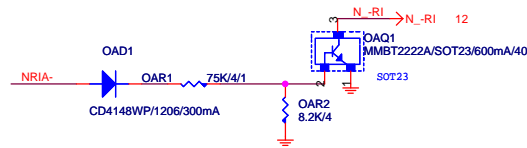
Sheet 18 of 34

Rev 1.02

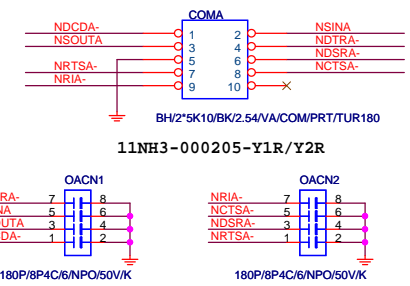
## COMA



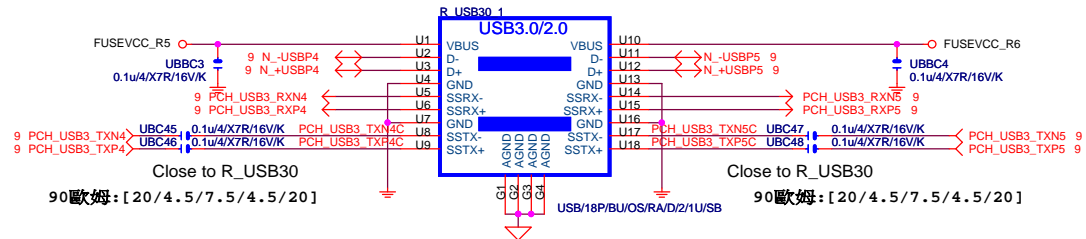
## COM RI



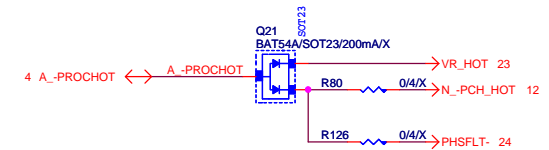
## COM BUFFER



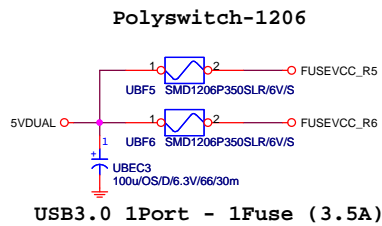
## USB30\_20 CONNECT



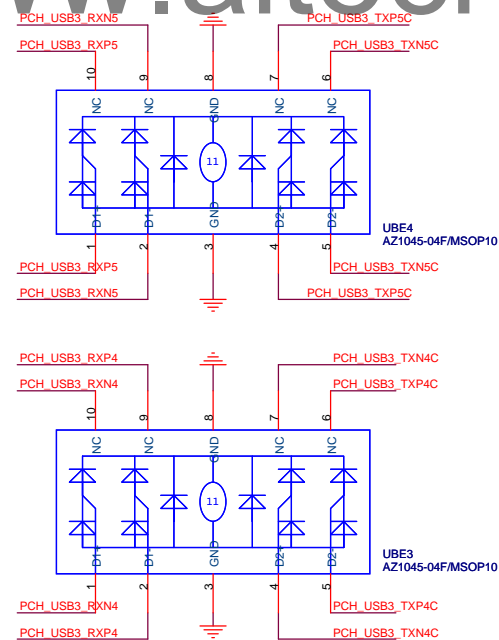
## -PROHOT



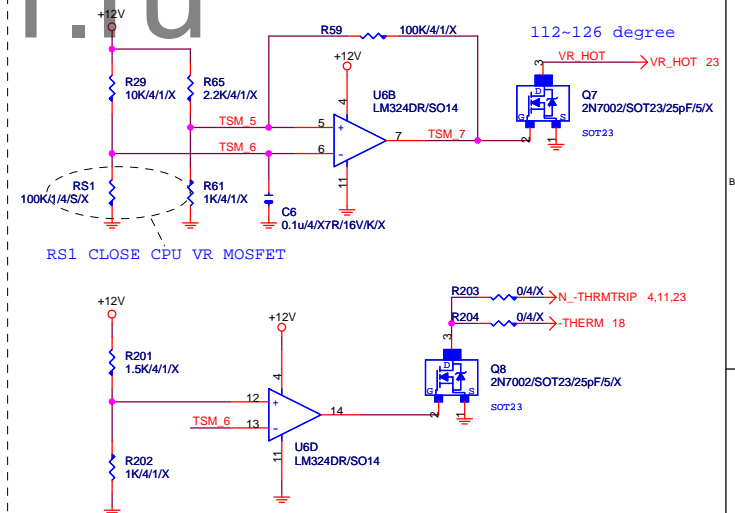
## USB30\_PWR



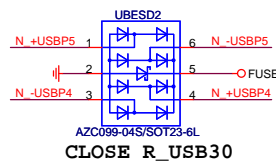
## USB30 ESD PROTECT



## -PROHOT



## USB20 ESD PROTECT

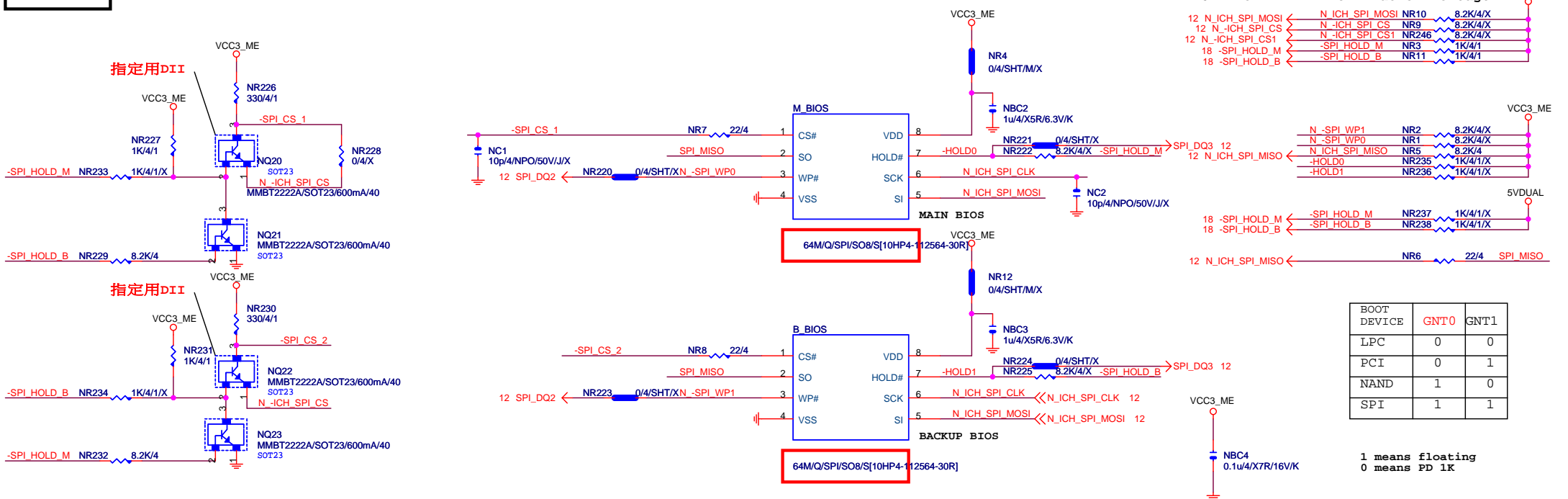


Gigabyte Technology

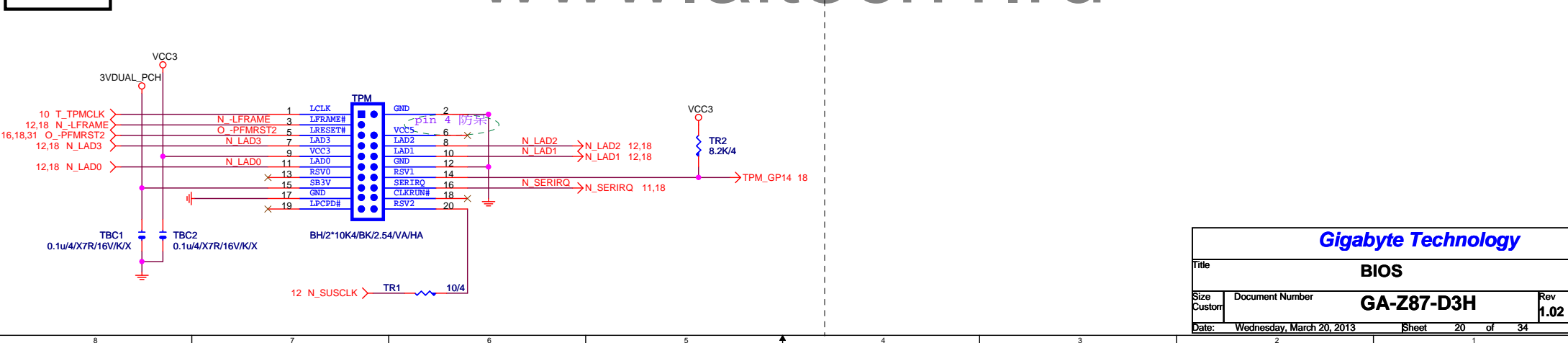
Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custom	GA-Z87-D3H	1.02	
Date:	Monday, March 18, 2013	Sheet	19 of 34

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DUAL BIOS

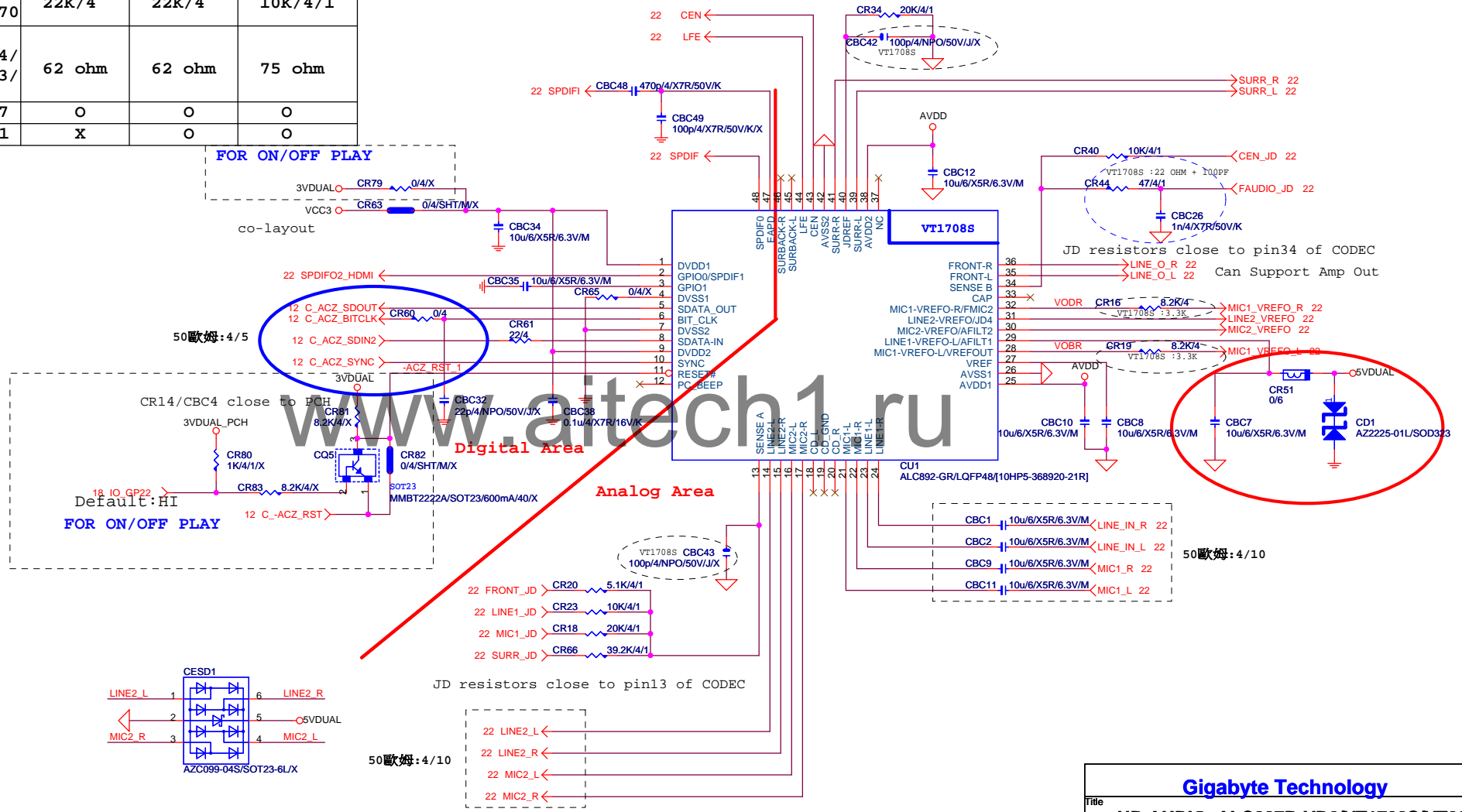


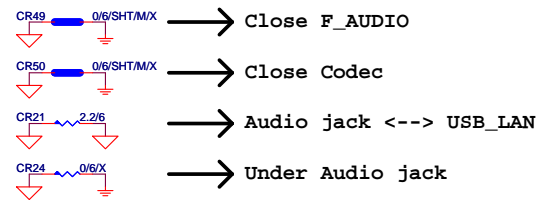
## TPM CONNECT



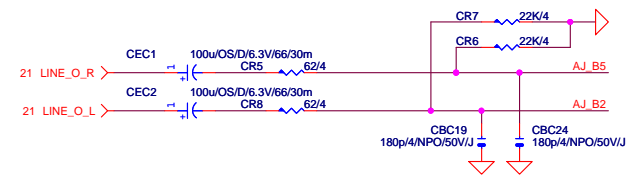


	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19			
CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/CR17/CR22/CR73/CR74/CR13/CR11/CR57/CR53/CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O



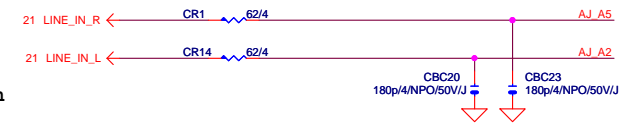


#### LINE-OUT



#### LINE-IN

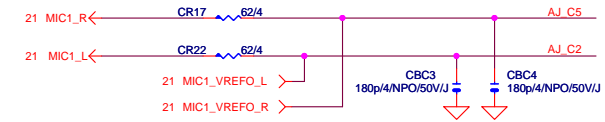
Only reserved for ALC888



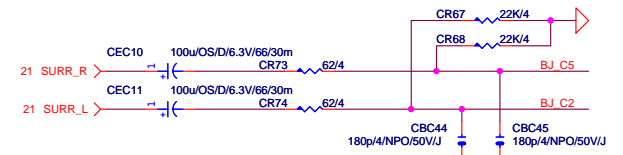
Verify MIC function  
in LINE-in

For 889A/888

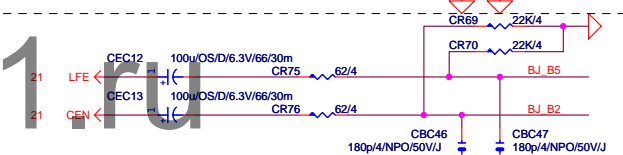
#### MIC-IN



#### SURROUND

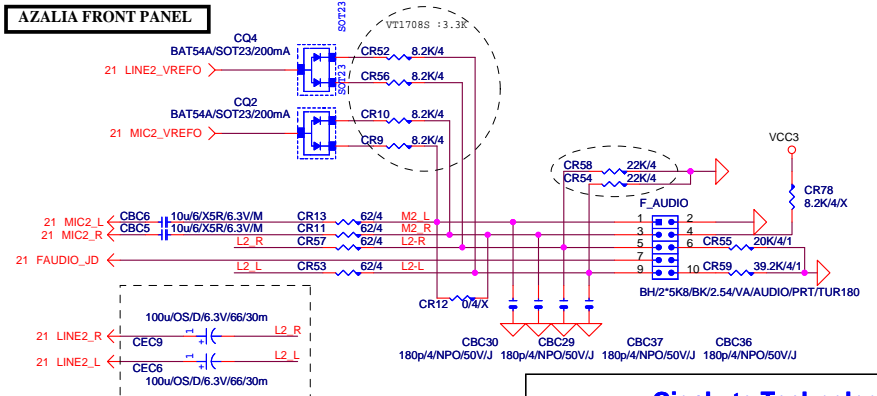


#### CEN/LFE



#### SURR BACK

#### AZALIA FRONT PANEL



Gigabyte Technology

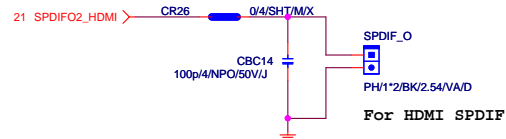
AUDIO JACK

GA-Z87-D3H

Rev 1.02

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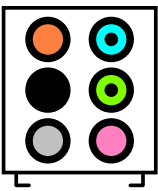
#### SPDIF\_OUT



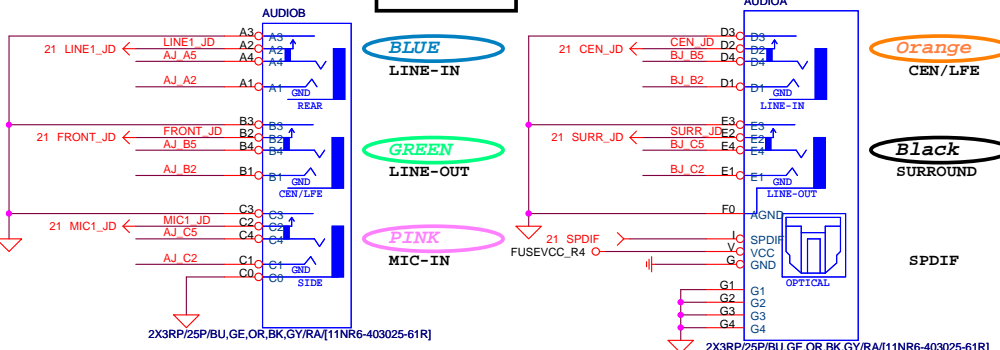
#### SPDIF\_IN

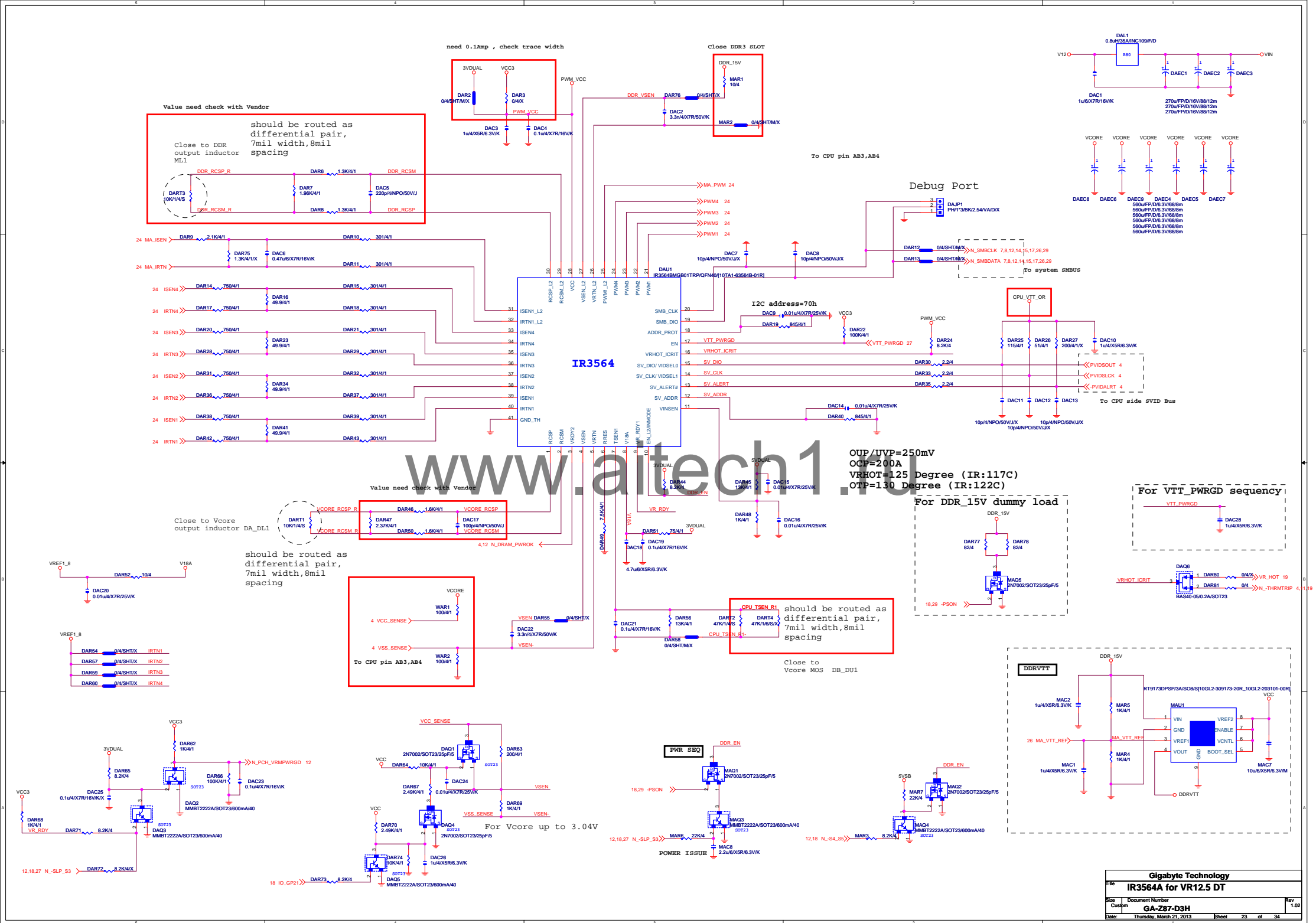


#### AZALIA JACK



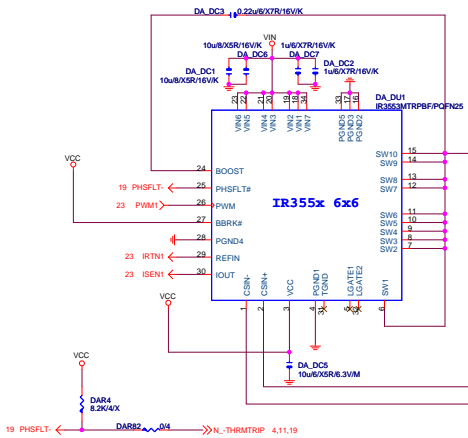
#### AZALIA JACK



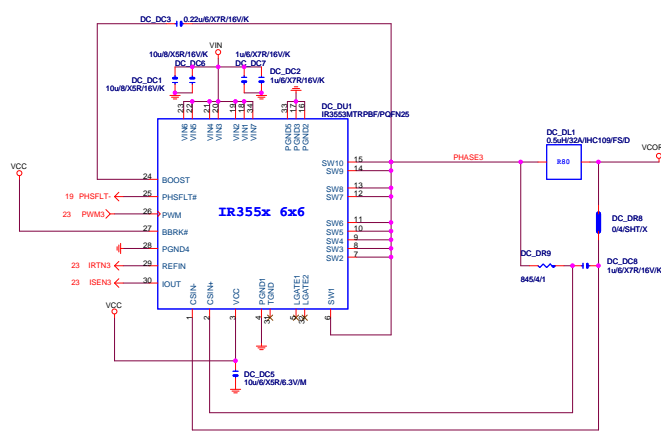


# VCORE

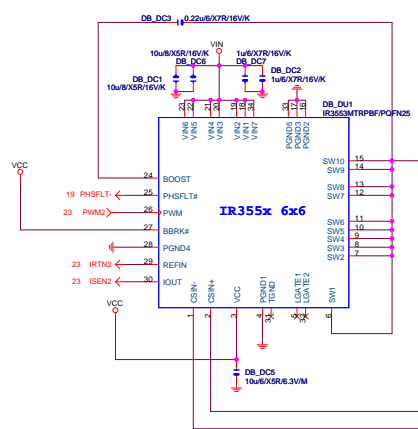
## VCORE-PHASE1



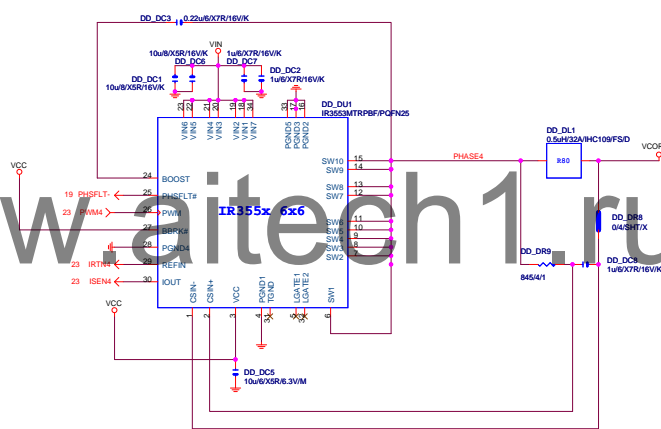
## VCORE-PHASE3



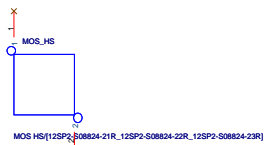
## VCORE-PHASE2



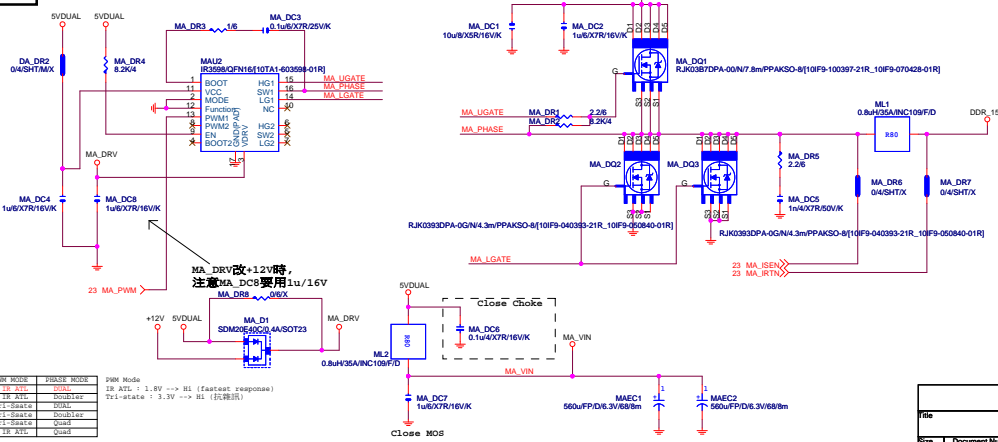
## VCORE-PHASE4



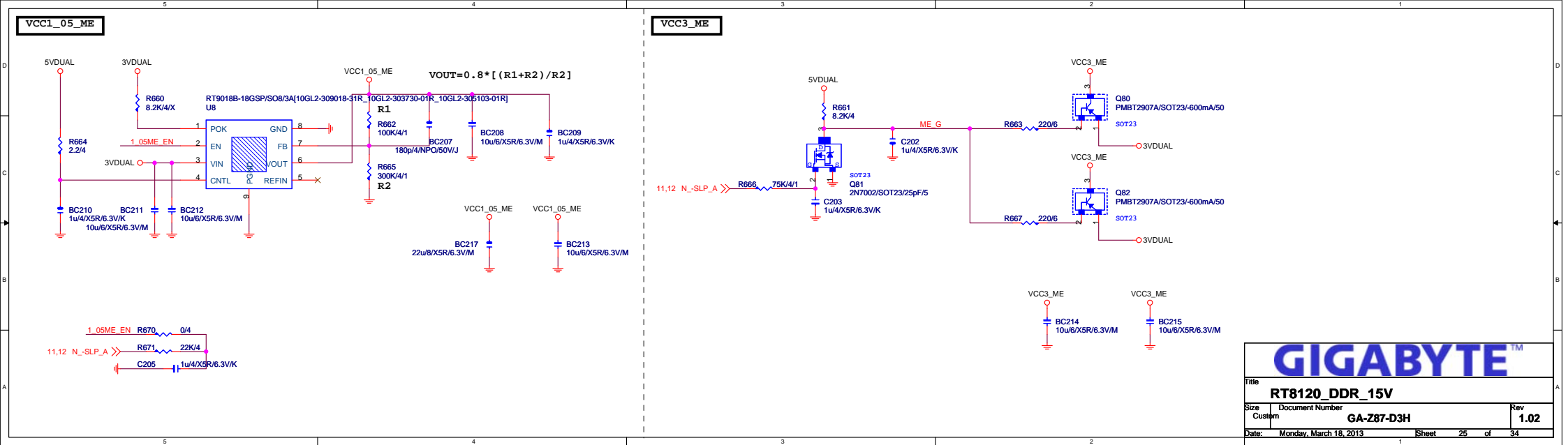
# MOSFET HEATSINK



# DDR\_15V

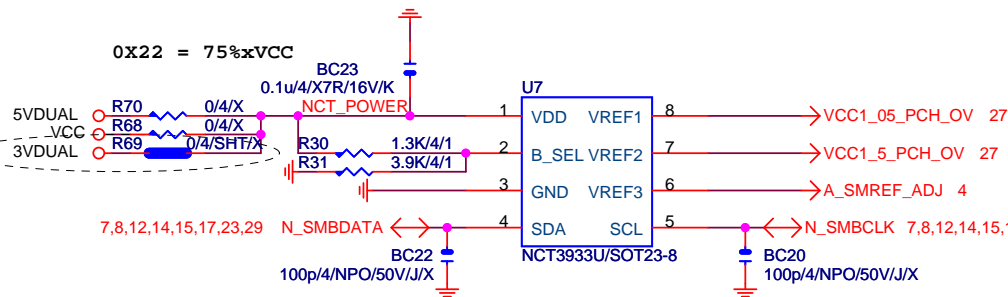


PHASE	MODE	PHASE	MODE
0	1	10	10
1	1	11	11
2	1	12	12
3	1	13	13
4	1	14	14
5	1	15	15
6	1	16	16
7	1	17	17
8	1	18	18
9	1	19	19

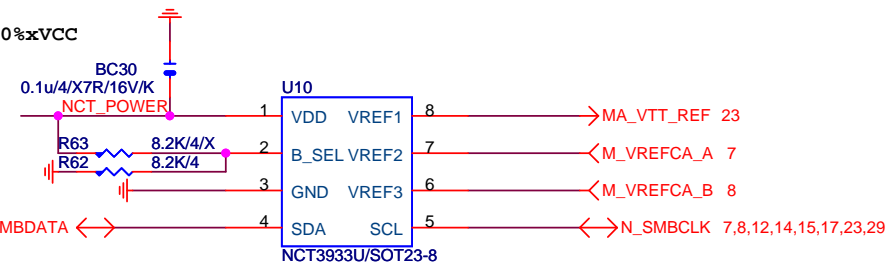


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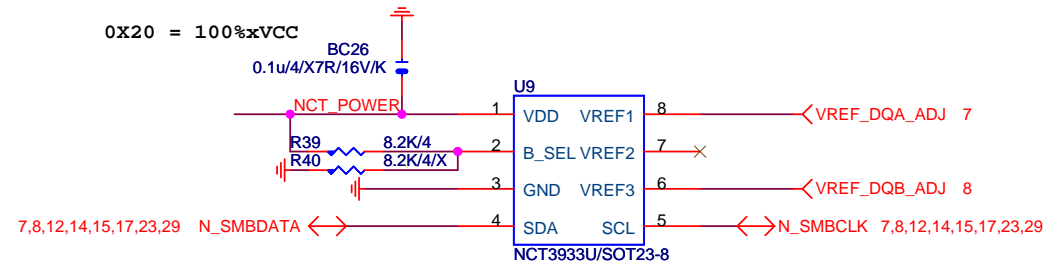
# OVER VOLTAGE



0X2A = 0%xVCC



0X20 = 100%xVCC



NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

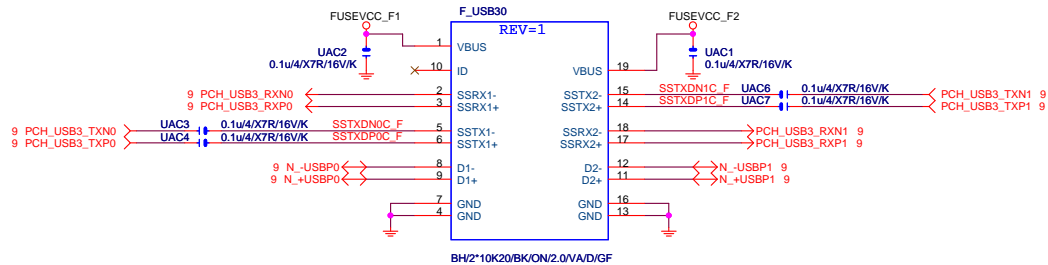
**Gigabyte Technology**

Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-Z87-D3H	1.02
Date:	Friday, March 15, 2013	Sheet 26 of 34

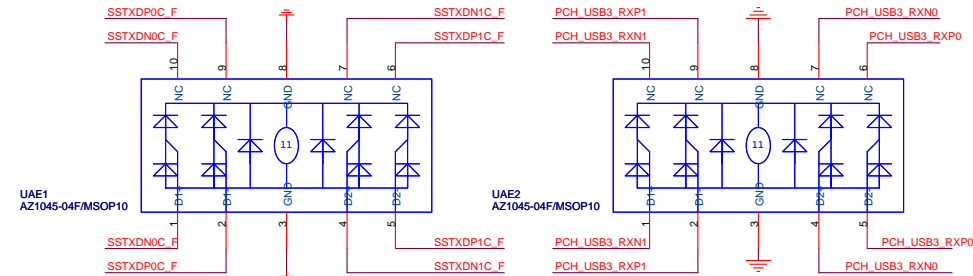




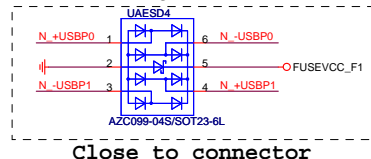
# Front USB3.0



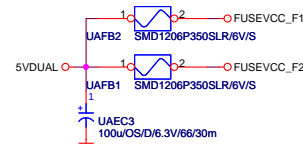
# F\_USB30 ESD PROTECT



# BLUE

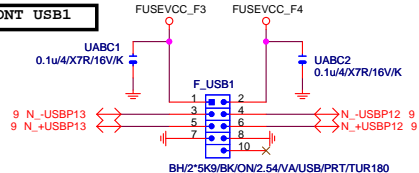


# F\_USB30 PWR

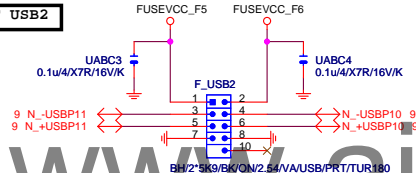


Close to connector

# FRONT USB1

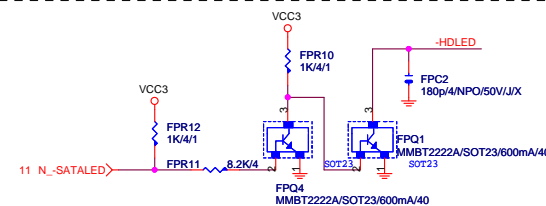


# FRONT USB2

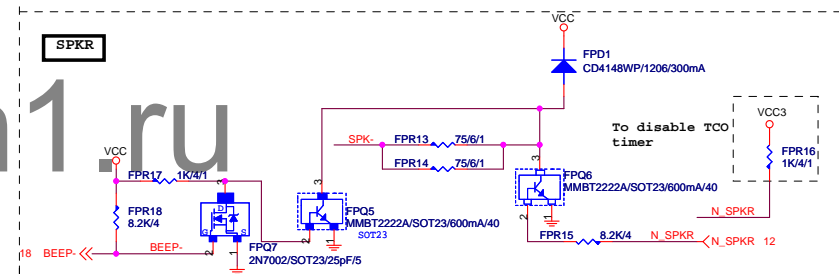


Close to connector

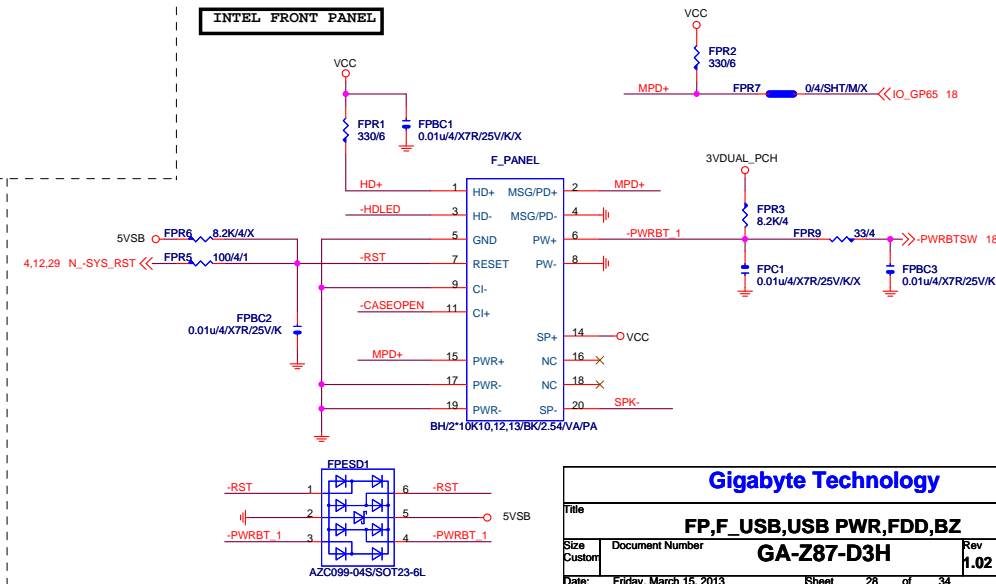
# SATA LED



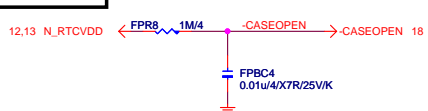
# SPKR



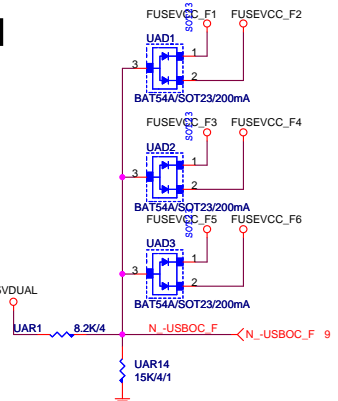
# INTEL FRONT PANEL



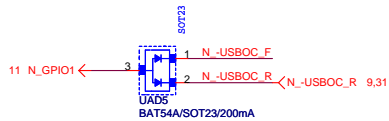
# CASE OPEN



# -USBOC\_F



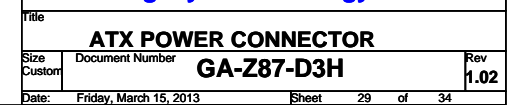
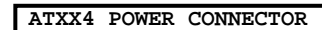
# F\_USB POWER PROTECT



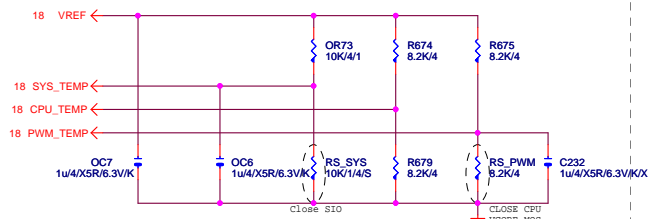
Gigabyte Technology

Title		FP,F_USB,USB PWR,FDD,BZ	
Size	Document Number	GA-Z87-D3H	
Custom	Rev	1.02	
Date	Friday, March 15, 2013	Sheet	28 of 34

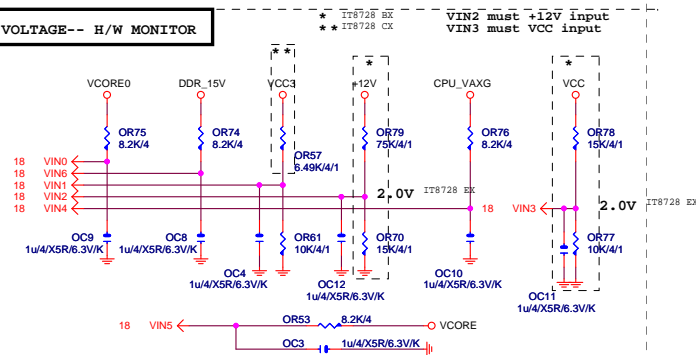
Patch some PSU no internal  
pull up resistor



## TEMP H/W MONITOR

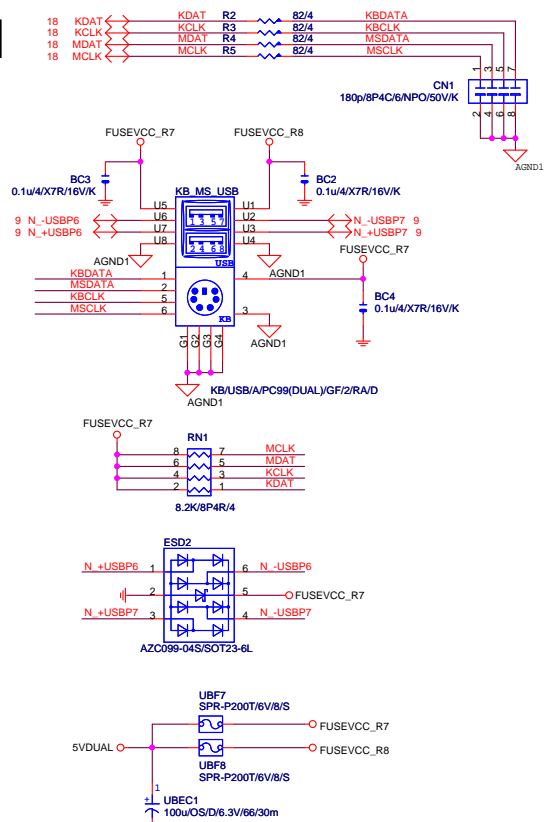


VOLTAGE-- H/W MONITOR

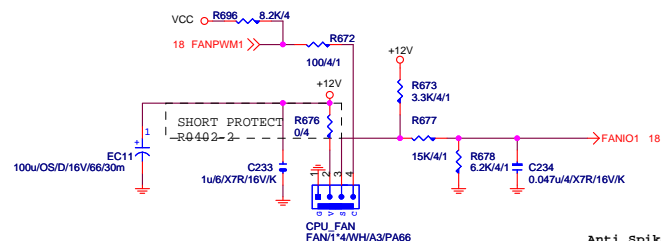


The division voltage of VIN2 & VIN3 must be around 2.9V

## KB/USB

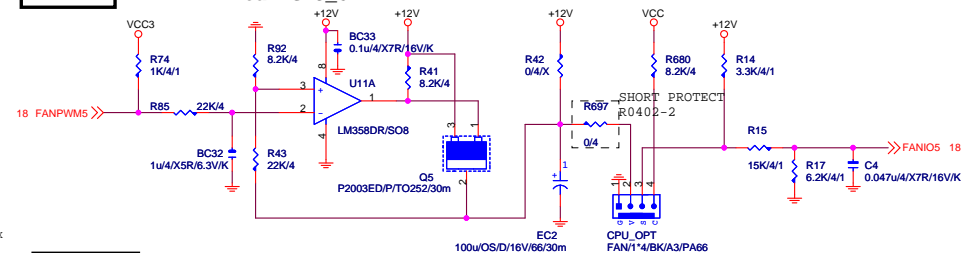


## CPU\_FAN



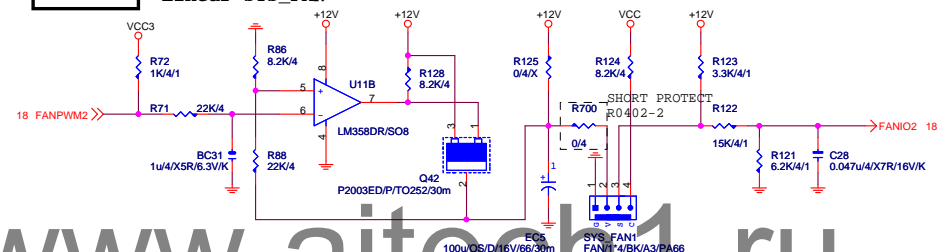
## CPU\_ OPT

## Linear CPU\_OPT



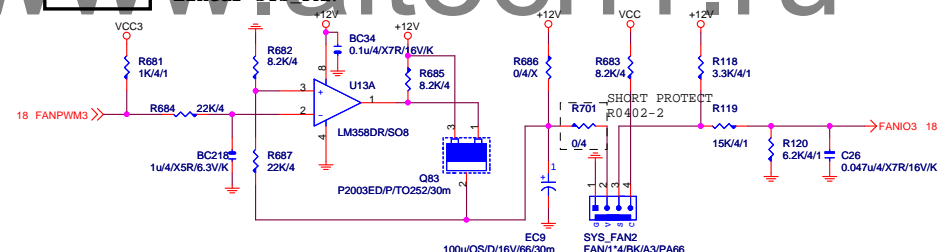
## SYS FAN\_1

Linear SYS\_FAN



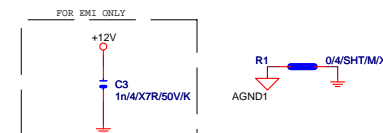
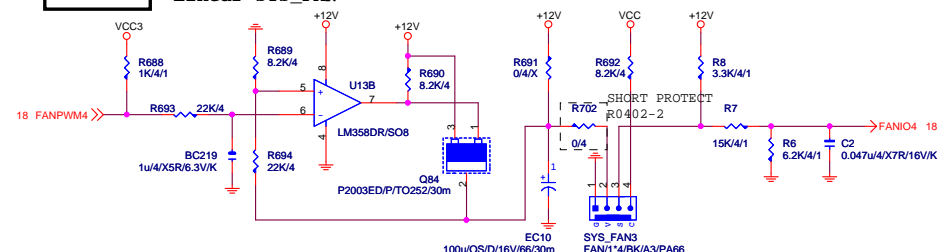
## SYS FAN\_2

Linear SYS FAN



## SYS FAN\_3

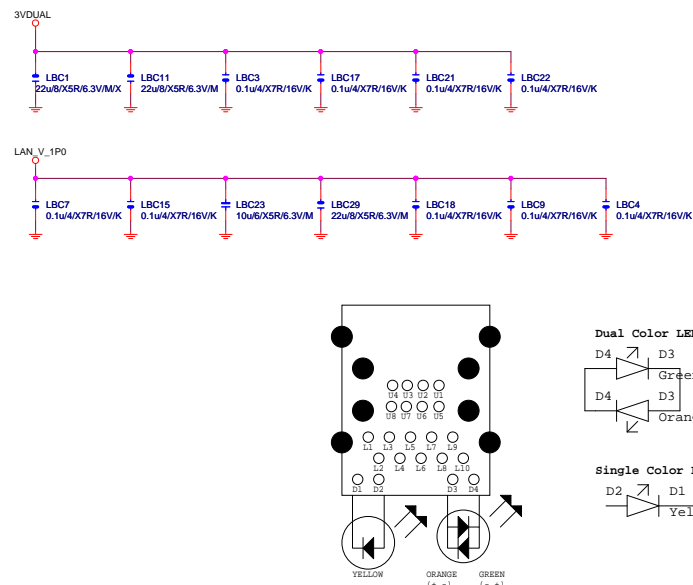
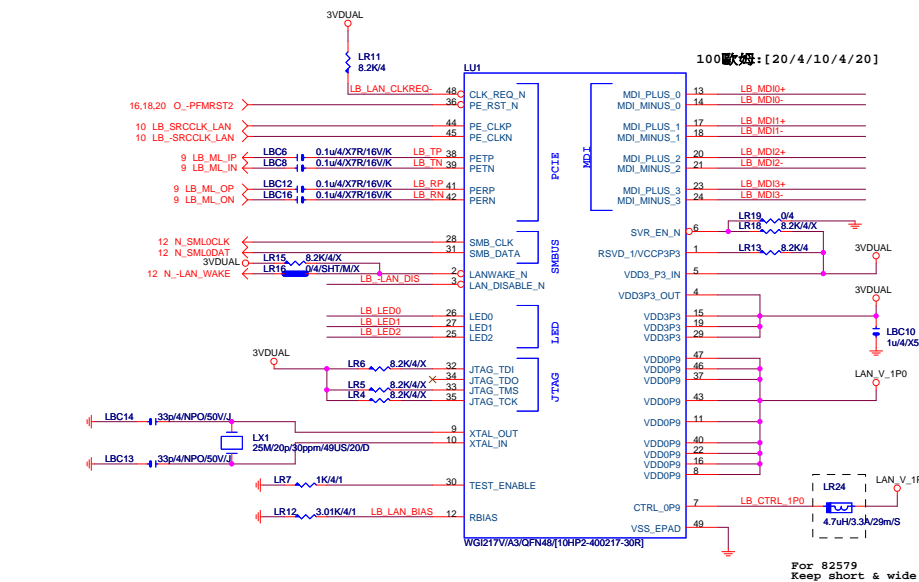
## Linear SYS\_FAN



## Gigabyte Technology

Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
Custom	GA-Z87-D3H	1.02	
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LAN:INTEL I217



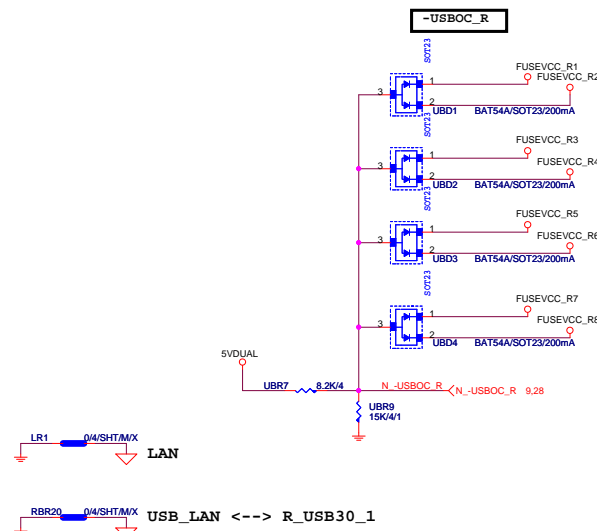
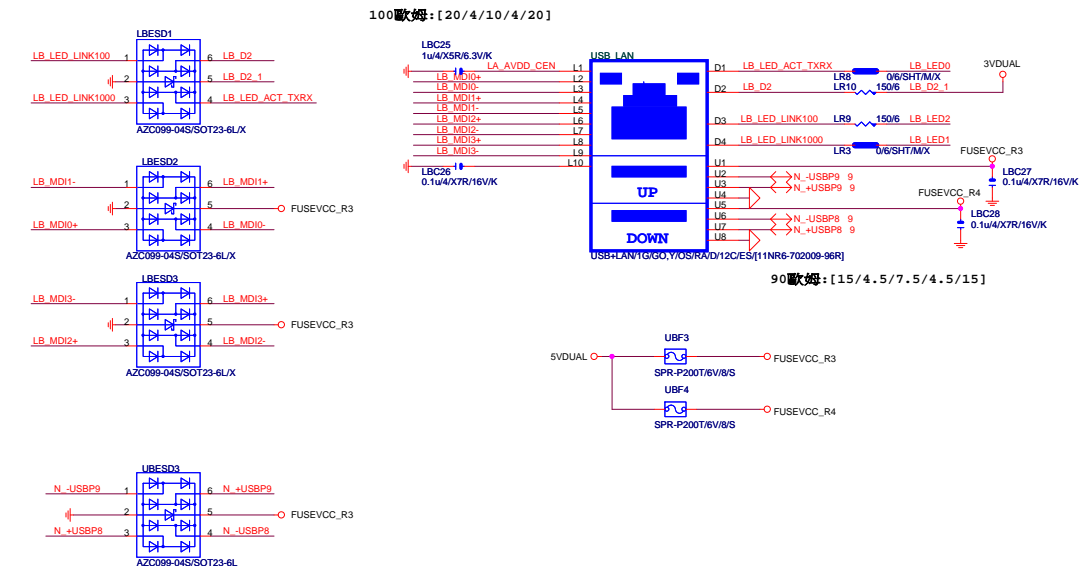
For 82579  
Keep short & wide

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1Gb	Orange
100Mb	Green
10Mb	Off

Access	Blinking
Link	Yellow

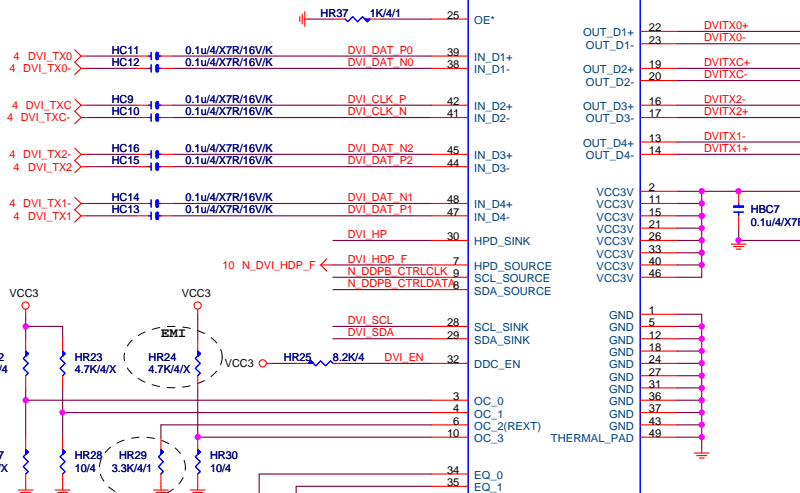
## USB30\_LAN CONNECTOR



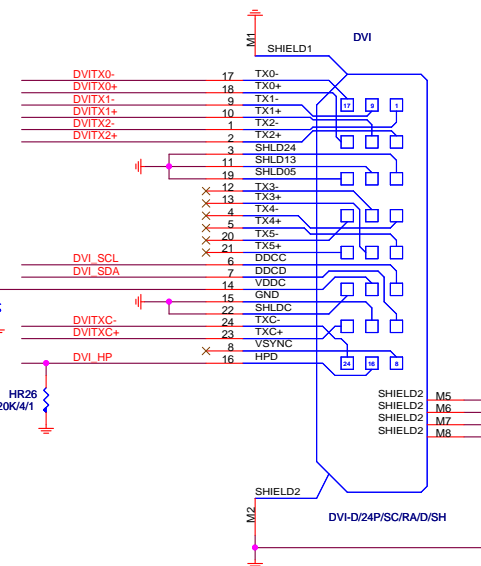
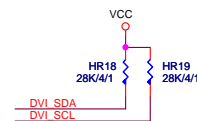
# DVI LEVEL SHIFT

DVI:15/4/4/15  
Impedance=85 +- 17.5%

HU2



10 N\_DDPB\_CTRLCLK <- N\_DDPB\_CTRLCLK  
10 N\_DDPB\_CTRLDATA <- N\_DDPB\_CTRLDATA



PERICOM 0/0/0/0:Vswing 500mV  
ASM1442  
DEFAULT 0/1/1 SWING:460mV -4dB

PI3DV411 0 0:3dB  
ASM1442 1 1:3dB

ASM1442/QFN48[10TA1-051442-20R]

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Gigabyte Technology

Title		
TI TSB43AB23 1394		
Size	Document Number	Rev
Custom	GA-H87-D3H	1.02
Date:	Thursday, March 28, 2013	Sheet 32 of 34

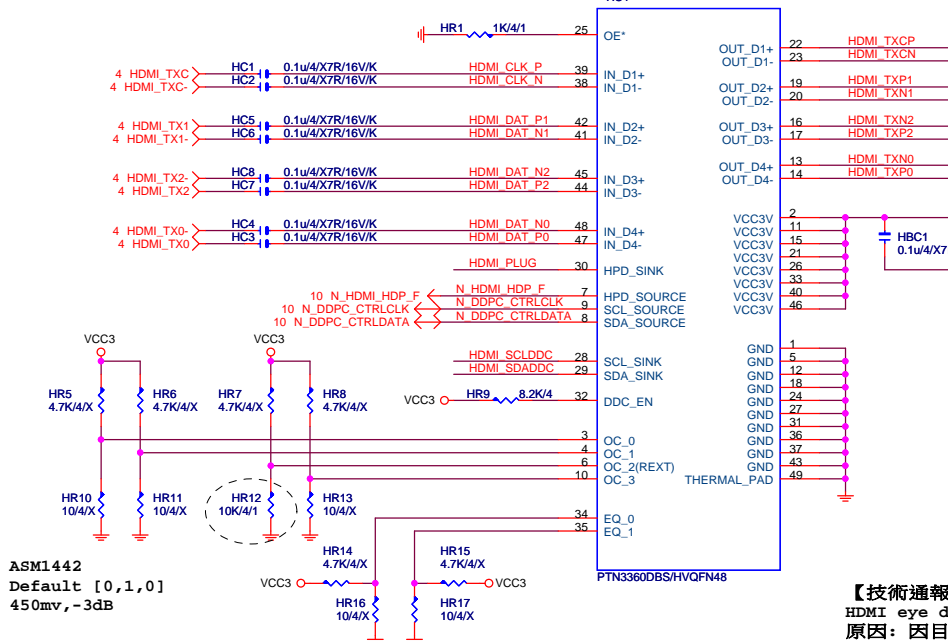


# HDMI LEVEL SHIFT

HDMI:15/4/4/15

Impedance=85 +- 17.5%

HU1



ASM1442  
Default [0,1,0]  
450mv, -3dB

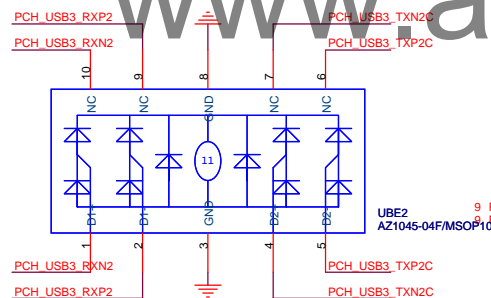
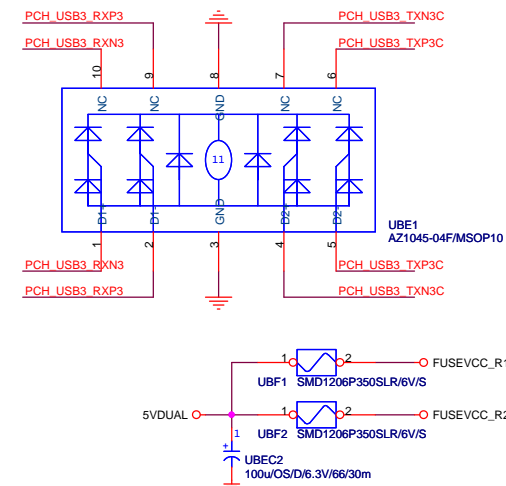
ASM1442 Default [0,0] 3dB  
[0,1]6dB

## 【技術通報R&D技術通報150】

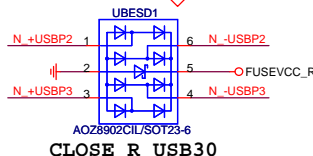
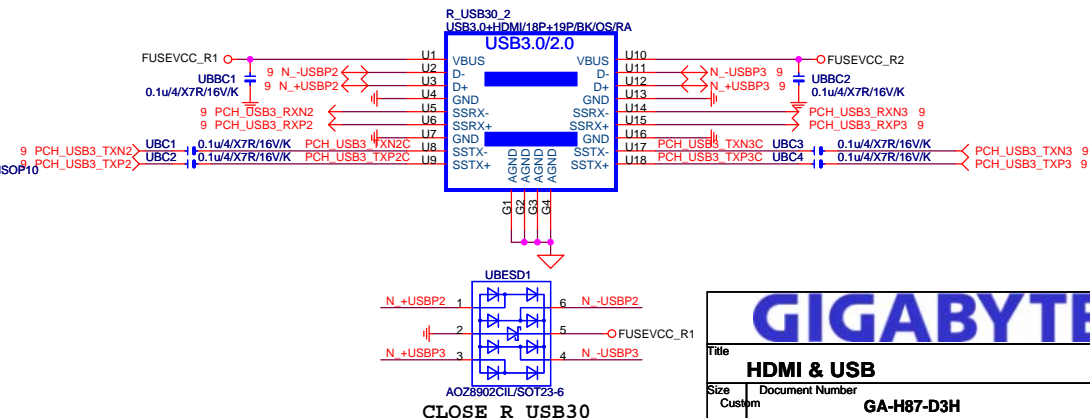
HDMI eye diagram1.4版(deep color)會fail

原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



## R\_USB30



GIGABYTE™			
HDMI & USB			
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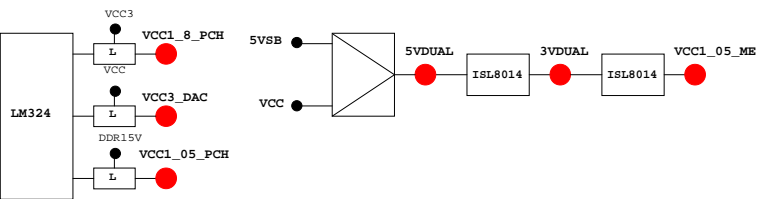
PCB GPIO LIST TABLE

PIN NAME	PWR	Default	USAG	NOTE
GP0	MAIN	H-Z	GPIO0	N/A
GP1/TACH1	MAIN	GPI	GPIO1	N/A
GP2/PIRQE#	MAIN	GPI	~PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	GPI	~PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	GPI	~PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	GPI	~PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN	GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8
GP9/OC5#	STBY	NATIVE	USB OC5#	N/A
GP10/OC6#	STBY	NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY	NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12
GP13	STBY	L	GPI	LPCPME#
GP14/OC7#	STBY	NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)
GP16	MAIN	GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN	GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN	GPI	Mobile Only	N/A
GP19	MAIN	GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN	GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN	GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22
GP23	MAIN	GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#
GP25	STBY		Mobile Only	N/A
GP26	STBY		Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27
GP28	STBY	H	GPO	PWR LED
GP29	STBY	L	GPI	GPIO29
GP30	STBY	H-Z	GPI	Mobile Only
GP31	STBY	H-Z	GPI	Mobile Only
GP32	MAIN	H	GPO	N/A
GP33	MAIN	H	GPO	N/A
GP34	MAIN	H-Z	GPI	~PCI_STOP
GP35	MAIN	L	GPO	~ACZ_DET
GP36	MAIN	GPI	N/A	N/A
GP37	MAIN	GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect
GP39	MAIN	H-Z	GPI	GPIO39
GP40	STBY	NATIVE	USB OC1#	N/A
GP41	STBY	NATIVE	USB OC2#	N/A
GP42	STBY	NATIVE	USB OC3#	N/A
GP43	STBY	NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44
GP45	STBY	NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46
GP47	STBY		Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48
GP49	MAIN	H-Z	IN	GPIO49
GP50	MAIN	NATIVE	~REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	~GNT1
GP52	MAIN	NATIVE	~REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	~GNT2
GP54	MAIN	NATIVE	~REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	~GNT3
GP56	STBY	NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1
GP58	STBY	H-Z	NATIVE	F_USB_OC
GP59	STBY	NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)
GP61	STBY	L	NATIVE	~SUSTAT
GP62	STBY	L	NATIVE	SUSCLK
GP63	STBY	L	NATIVE	GPIO63
GP64	MAIN	L	NATIVE	CLKOUTFLEX0
GP65	MAIN	L	NATIVE	CLKOUTFLEX1
GP66	MAIN	L	NATIVE	CLKOUTFLEX2
GP67	MAIN	L	NATIVE	CLKOUTFLEX3
GP72	STBY	H-Z	NATIVE	VCORE_OV4
GP73	STBY		Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2
GP75	STBY	H-Z	NATIVE	N/A(Reverse)

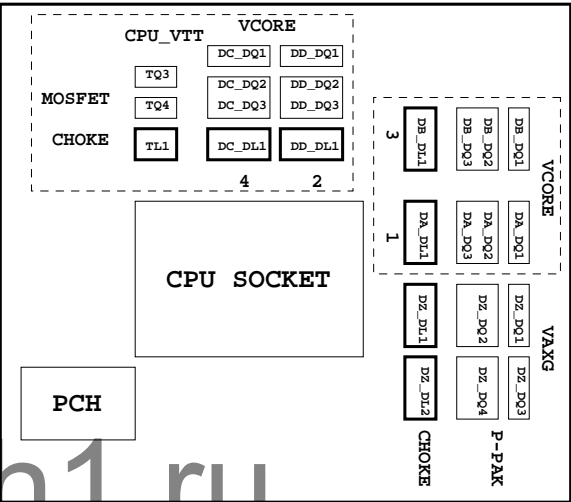
Super I/O ITE8720 GPIO Table

PIN NAME	USAG	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAG	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SEN	LOW_PWR_1	
VIDO5/GP27/SEN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	SEN_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

散熱模組料號:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
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